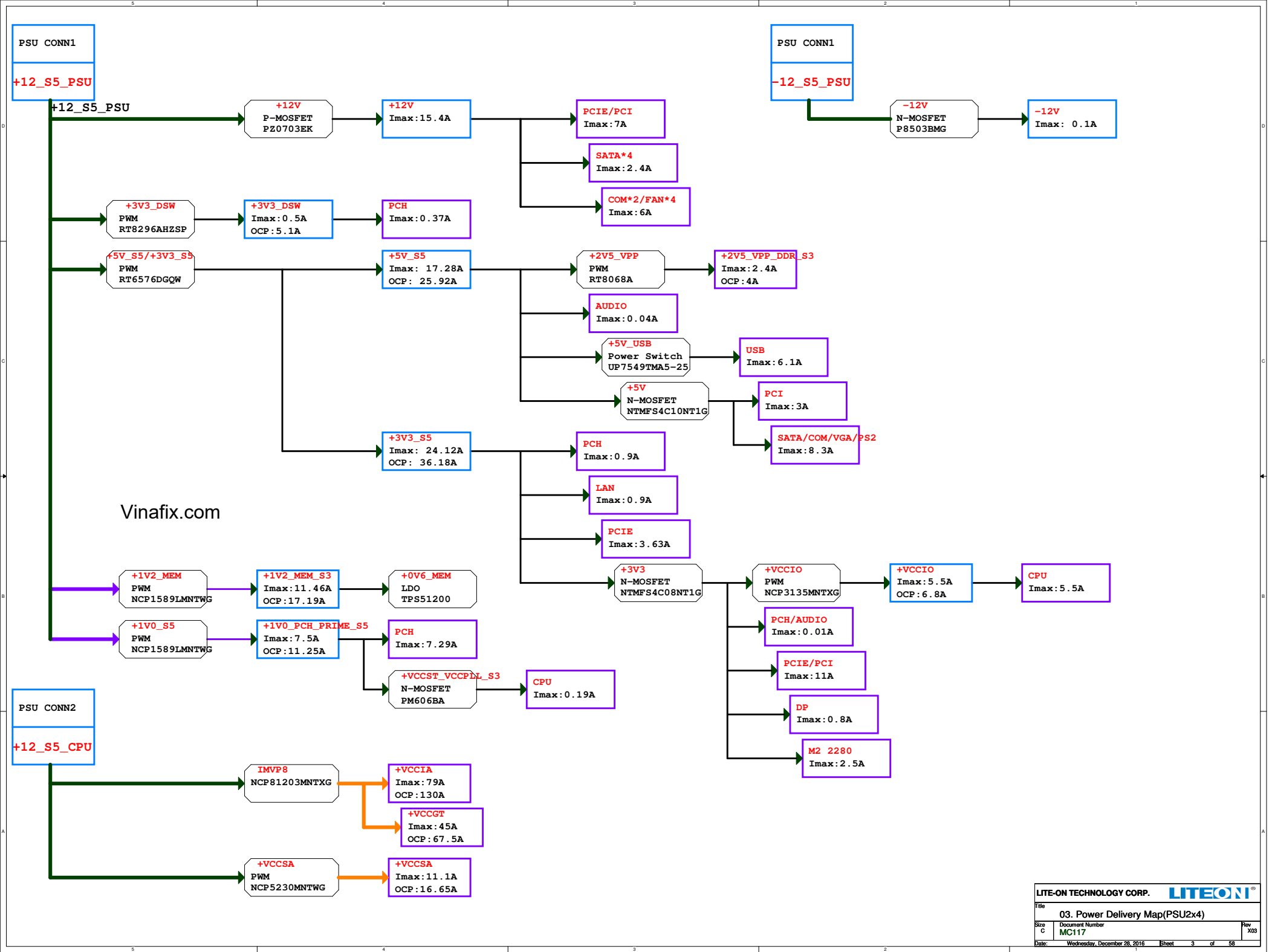
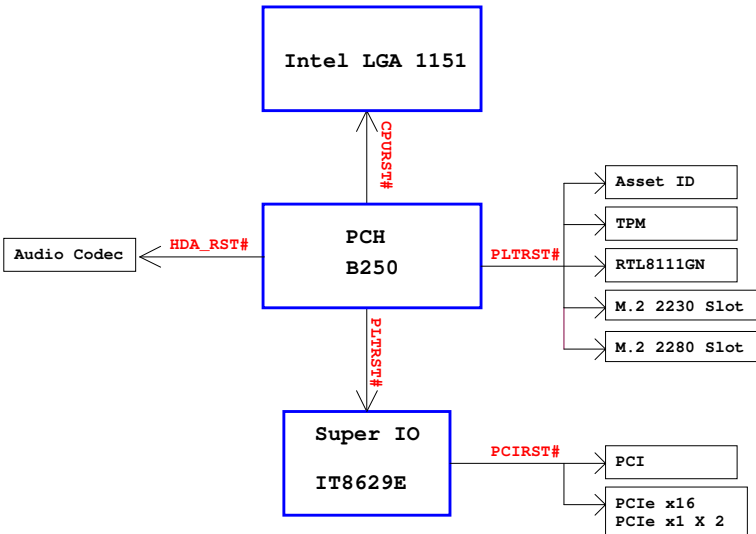


PAGE	TITLE
01	Block Diagram
02	Power Sequence
03	Power Delivery Map(PSU2x4)
04	RESET/CLOCK MAP/SMBus
05	Strapping Pin
06	KABYLAKE-DDR
07	KABYLAKE-PEG/DMI/DDI/EDP
08	KABYLAKE-POWER/+VCCST
09	KABYLAKE-CPU CORE/GPU CORE
10	KABYLAKE-VSS
11	KABYLAKE-CFG/XDP
12	CPU XDP CONNECTOR
13	PCH-SPI/GPIO
14	PCH-USB2.0/PCIE/SATA/PCIE
15	PCH-AUDIO/SMBUS/RTC
16	PCH-GPIO
17	PCH-USB3/LPC/CLK
18	PCH-POWER
19	PCH-VSS
20	PCH-STRAPS
21	DSW*
22	PWRGD & Bleed Off
23	DDR4 CHA UDIMM1
24	DDR4 CHA UDIMM2
25	DDR4 CHB UDIMM3
26	DDR4 CHB UDIMM4
27	DP1/HDMI1
28	DP2/HDMI2
29	DP to VGA(IT6516B)
30	PCIe X16 / X1 SLOT
31	PCI Bridge(IT8893)
32	M2 WIFI/SSD
33	Audio Codec(ALC662)
34	LAN(RTL8111GN)/USB Debug
35	SIO(IT8629E)
36	TPM2.0
37	Rear USB3.0
38	Front USB3.0/USB Charger
39	USB2.0 Header
40	FAN/SATA
41	COM PORT/PS2
42	LPT Pin Header
43	Asset ID
44	Button/LED
45	APS Debug Port/ATX PWROK
46	SM BUS/Thermal Sensing/ATX
47	Mounting Hole
48	+3V3 DSW / -12V
49	+5V_S5/+3V3_S5
50	+5V / +3V3
51	VCORE CONTROLLER
52	VCCIA Output
53	VCCGT Output
54	+1V2 DDR/+0V6_VTT
55	+2V5_VPP_DDR
56	+1V0_PCH_PRIME
57	+VCCIO
58	+VCCSA
59	
60	
61	
62	



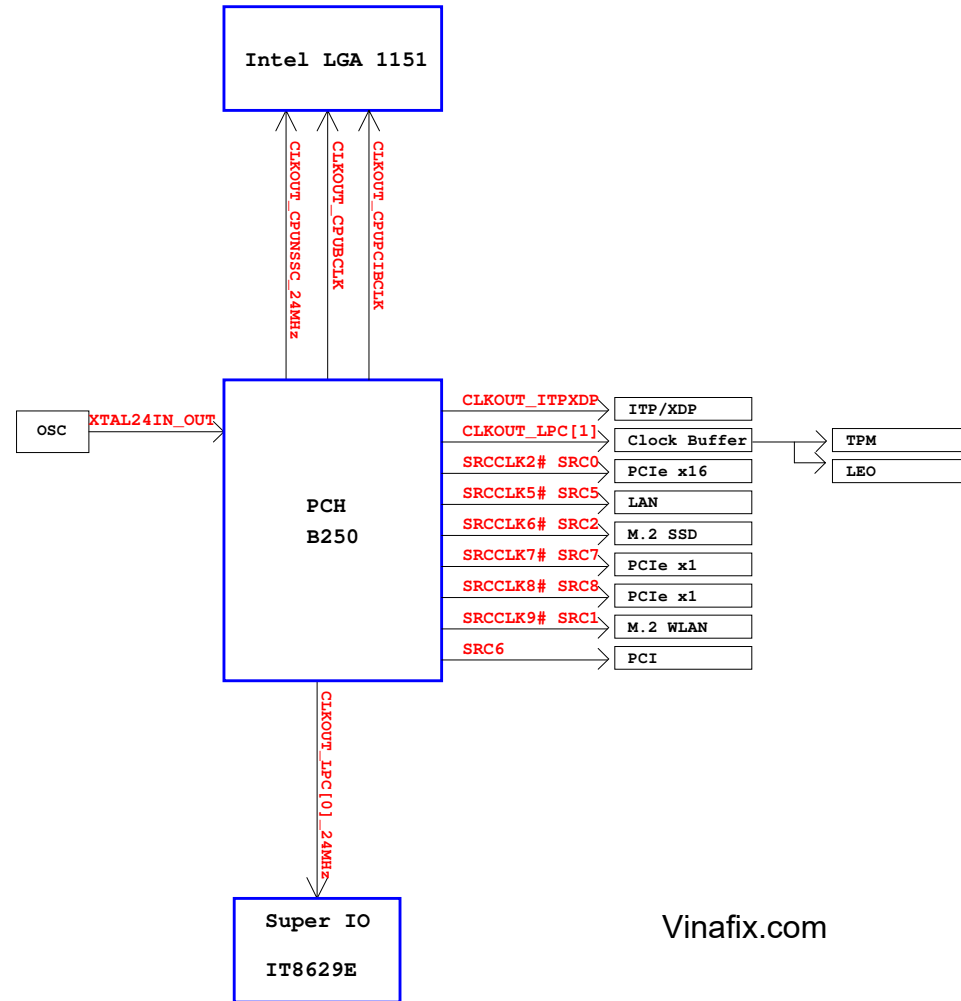
RESET MAP



SMBUS table

Signal	Communication
SMBCLK & SMBDATA	PCIe x16, PCIe x1, PCI, M.2 WLAN, DDR4, Asset ID
SML0CLK & SML0DATA	LAN(reserve)
SML1CLK & SML1DATA	Super IO

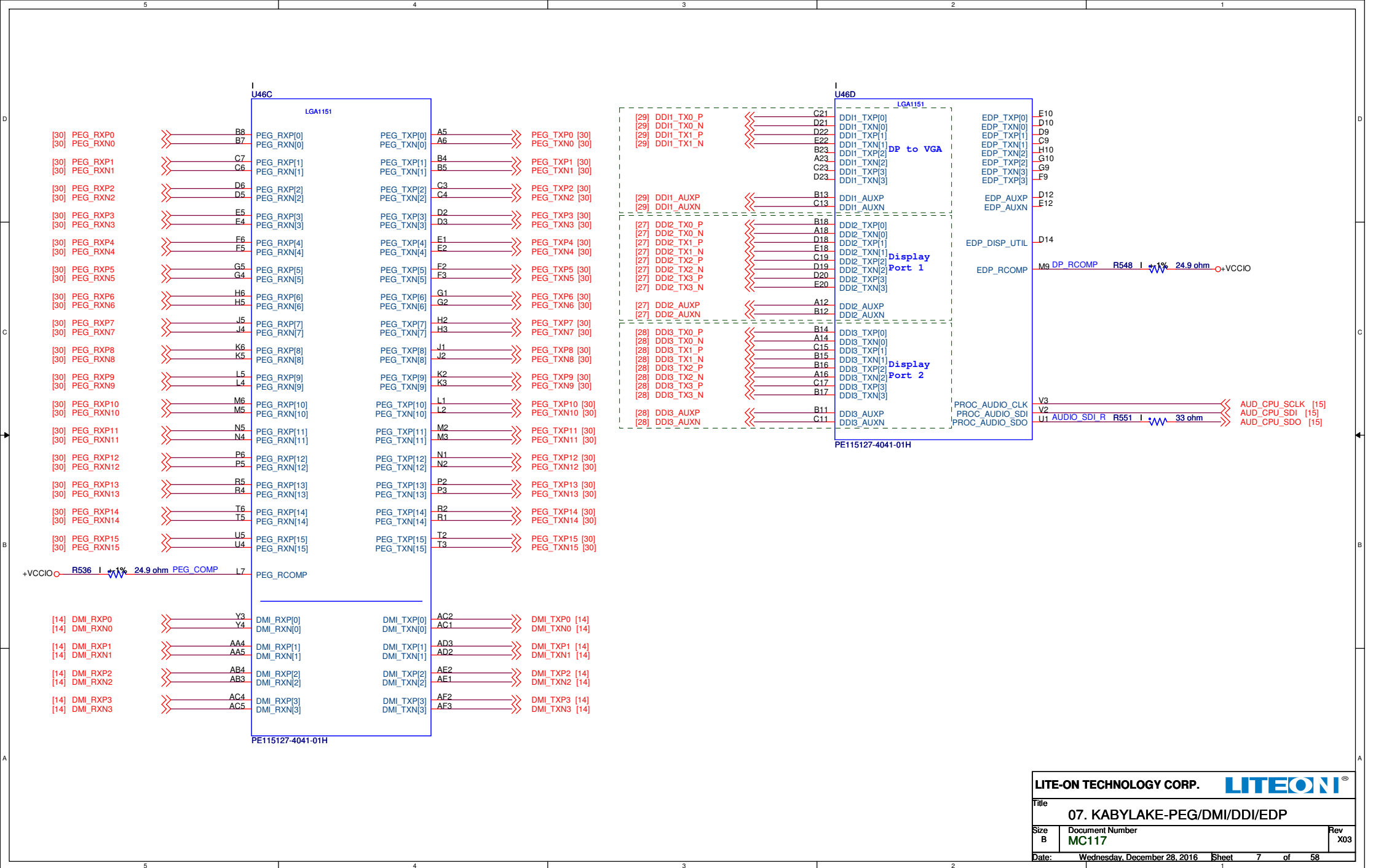
CLOCK DIAGRAM

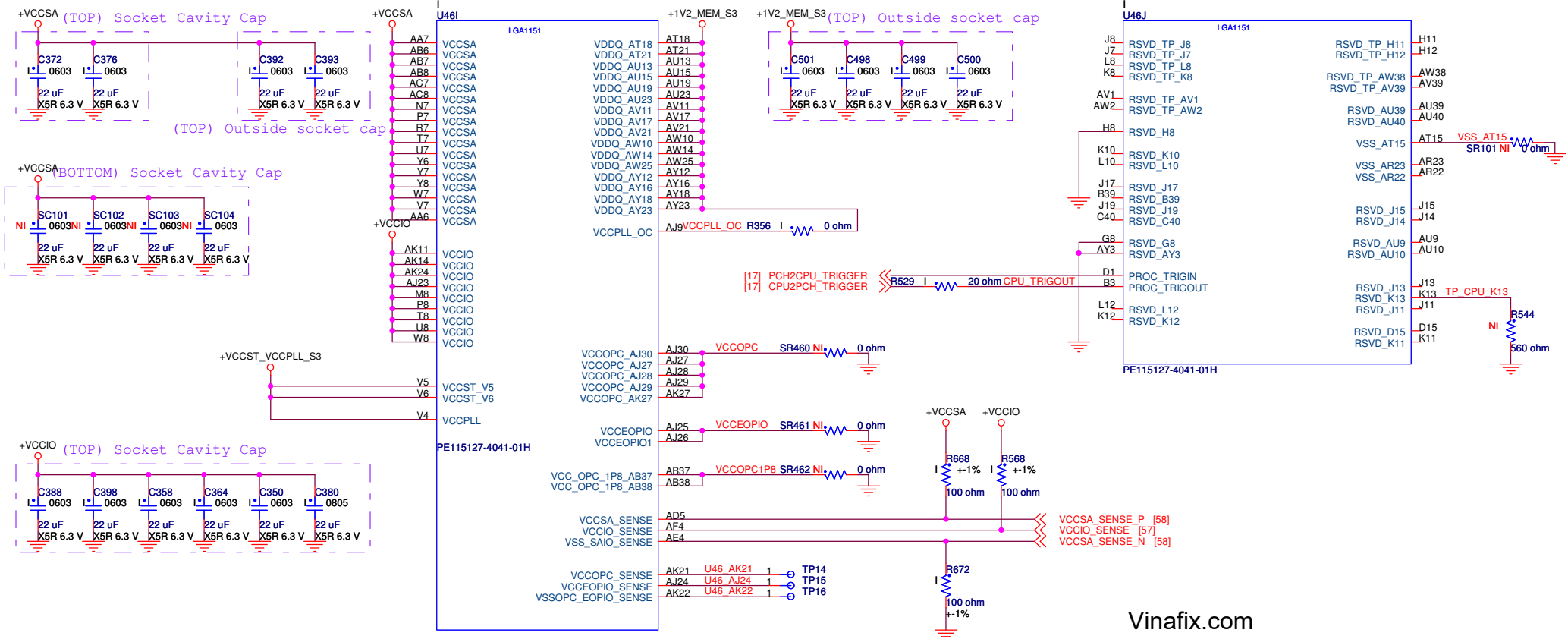


Vinafix.com

STRAPPING PIN

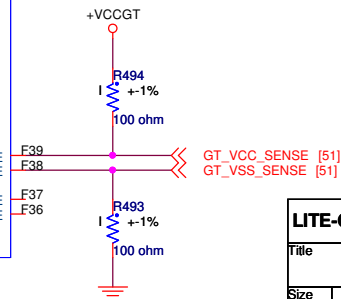
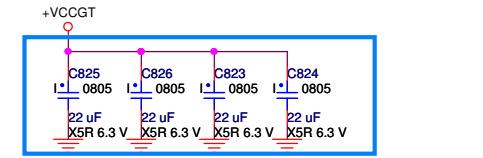
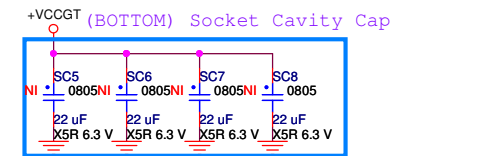
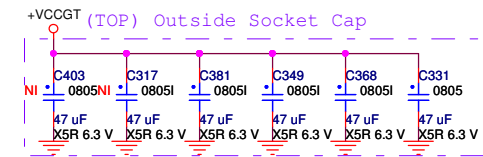
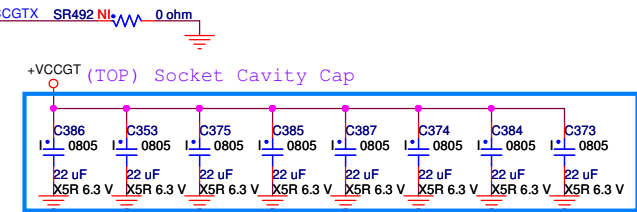
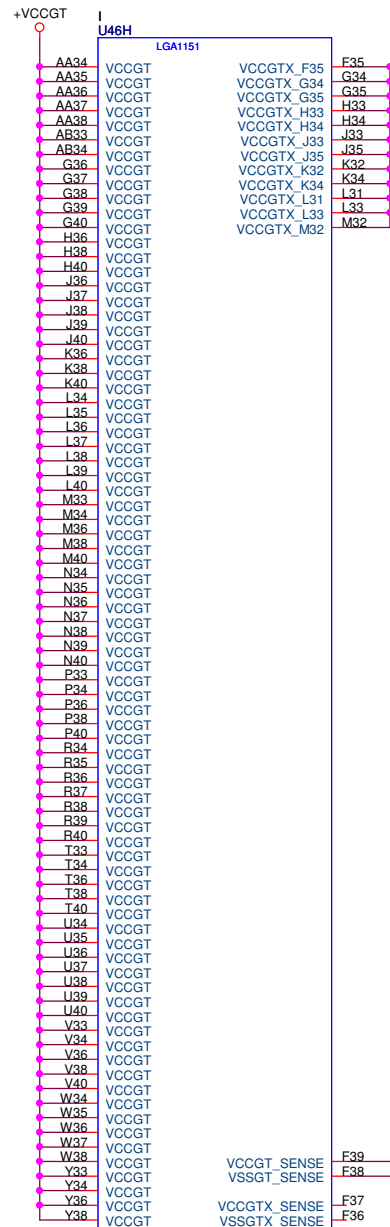
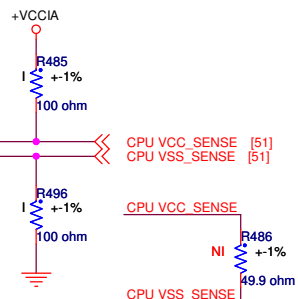
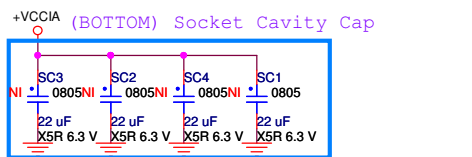
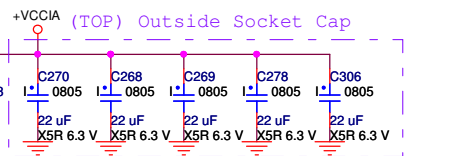
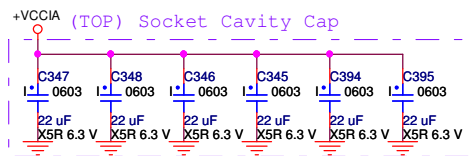
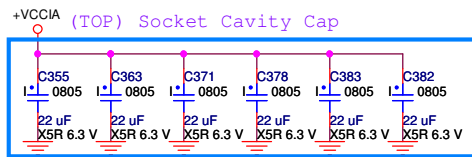
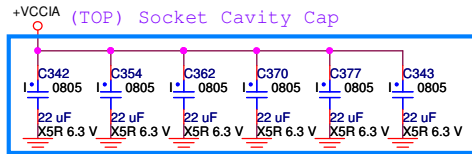
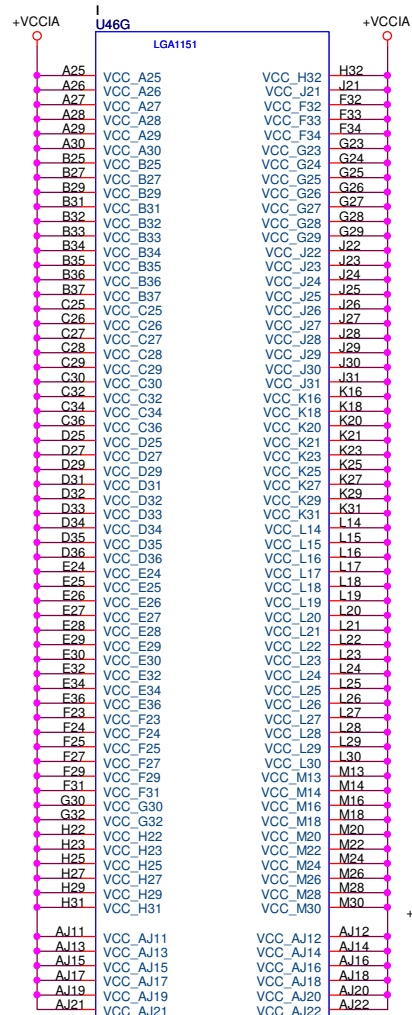
Signal	Usage	When Sampled	Comment
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable Top Swap mode. (Default) 1 = Enable Top Swap mode.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable(default) No Reboot mode. 1 = Enable No Reboot mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
SMBALERT# / GPP_C2	TLS Confi- dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).(default)
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. Bit 10 Boot BIOS Destination 0 SPI(default) 1 LPC
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC Is selected for EC.(default) 1 = eSPI Is selected for EC.
HDA_SDO	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. (reserve pull high)
DDPB_CTRLDATA / GPP_I6	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected.
DDPC_CTRLDATA / GPP_I8	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected.
DDPD_CTRLDATA / GPP_I10	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected.





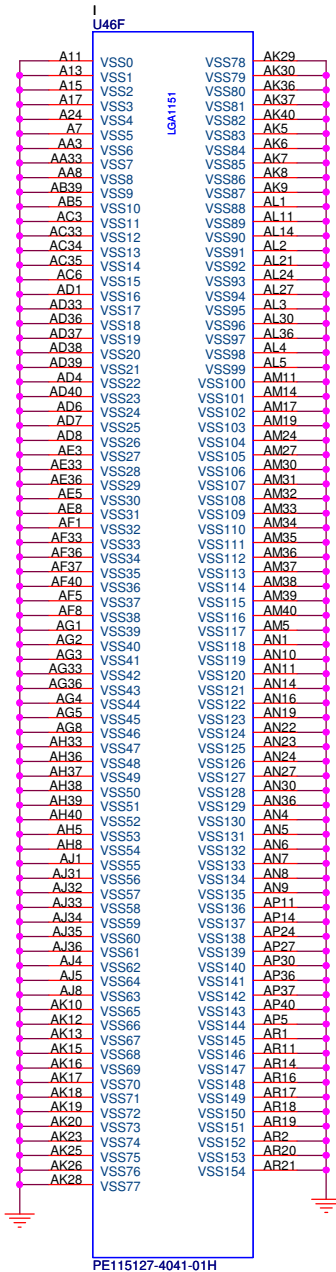
Vinafix.com

LITE-ON TECHNOLOGY CORP. LITEON		
Title		
08. KABYLAK-POWER/+VCCST		
Size	Document Number	Rev
B	MC117	X03
Date:	Wednesday, December 28, 2016	Sheet 8 of 58

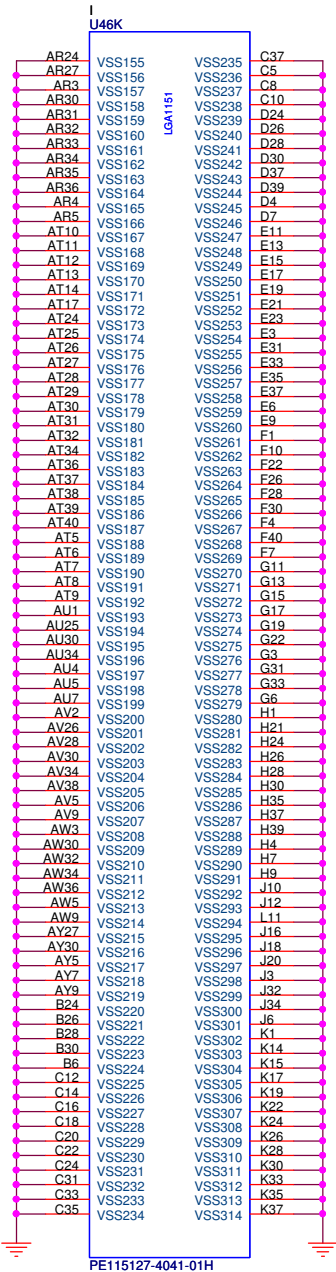


Vinafix.com

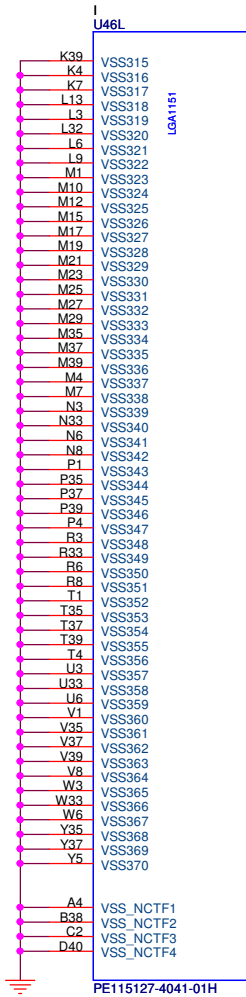
LITE-ON TECHNOLOGY CORP. LITEON®		
Title		
09. KABYLAK-CPU CORE/GPU CORE		
Size	Document Number	Rev
B	MC117	X03
Date:	Wednesday, December 28, 2016	Sheet 9 of 58



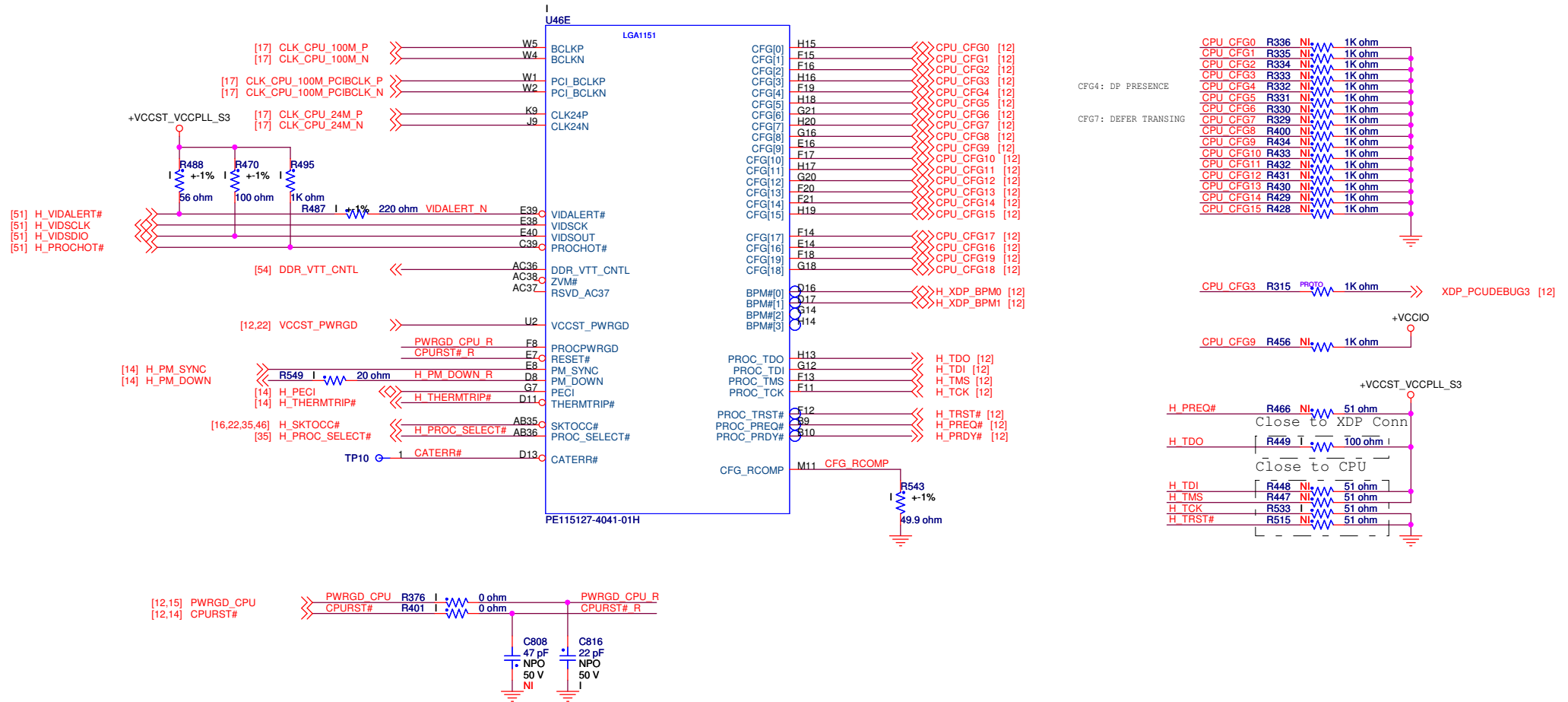
PE115127-4041-01H



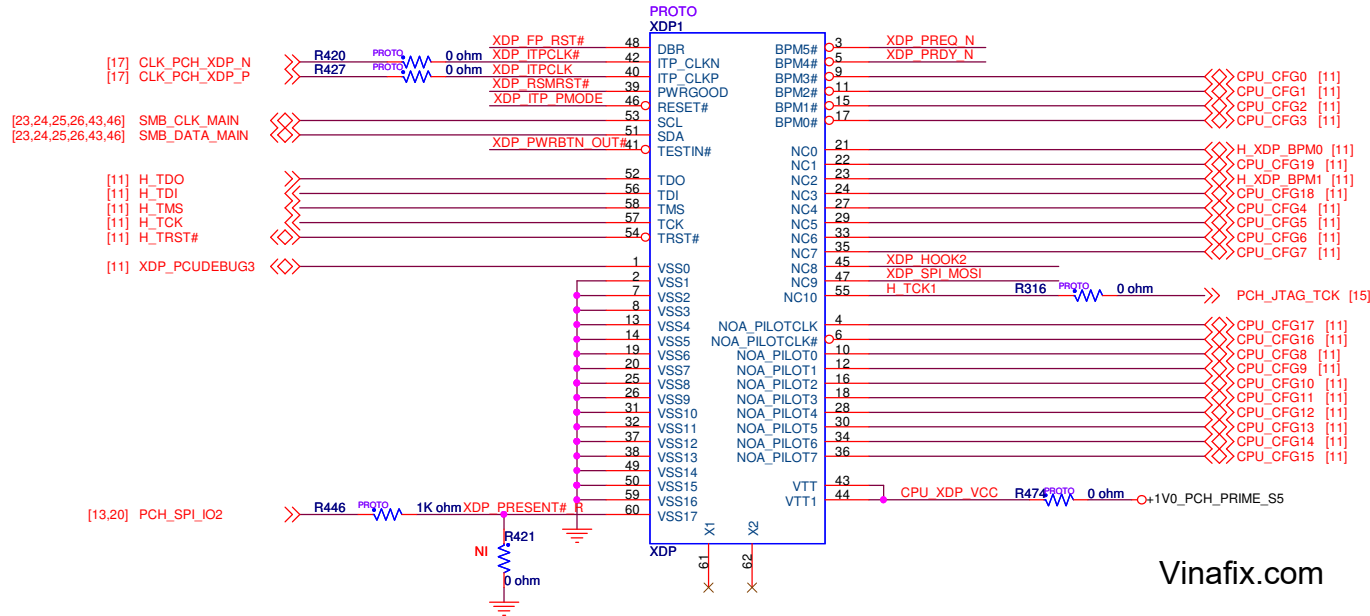
PE115127-4041-01H



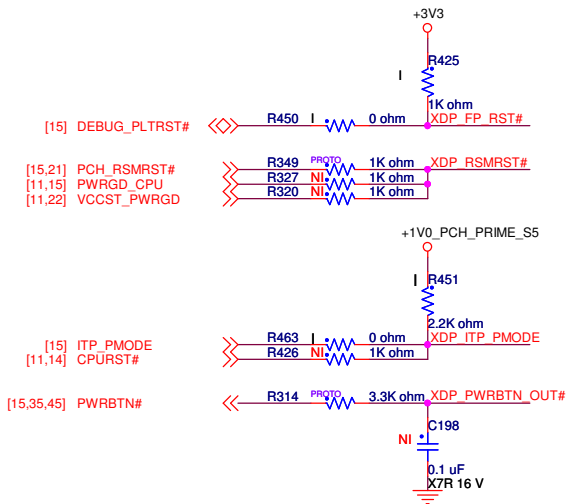
LITE-ON TECHNOLOGY CORP.		LITEON [®]	
Title			
10. KABYLAKES-VSS			
Size	Document Number	Rev	
B	MC117	X03	
Date:	Wednesday, December 28, 2016	Sheet	10 of 58



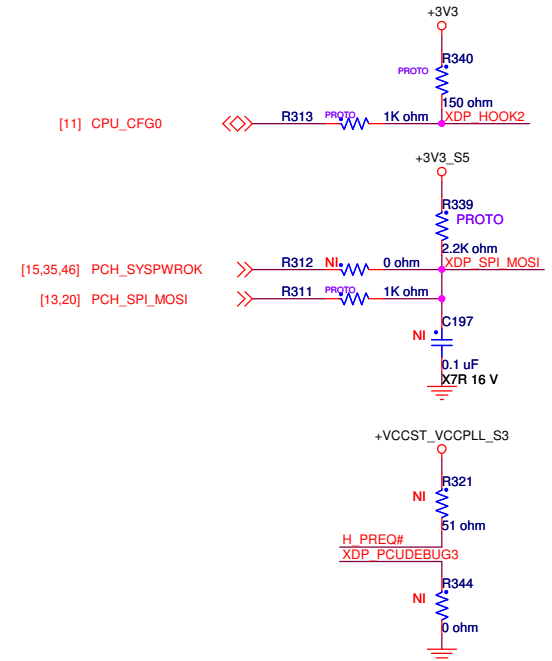
Intel XDP Debugging Connector

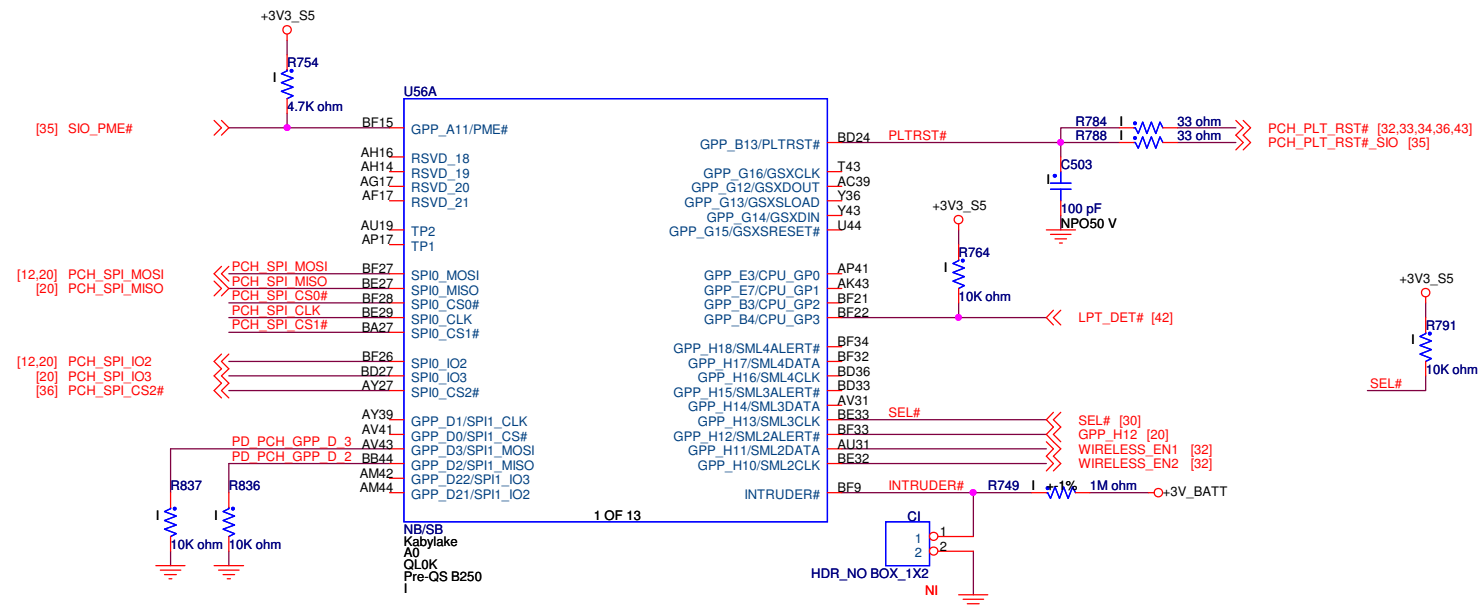


Vinafix.com

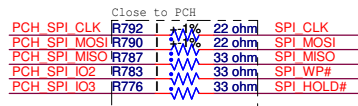


Bifurcation	Link Width			Config. Signals			Lanes																
	0:1:0	0:1:1	0:1:2	CFG [6]	CF G [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1x16 Reversed	x16	N/A	N/A	1	1	0	1	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3	
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0	



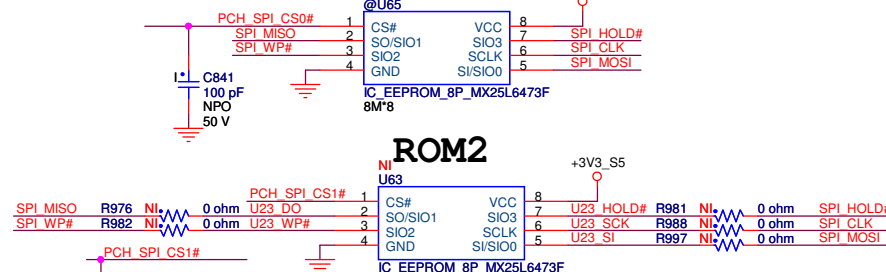


SPI SOCKET



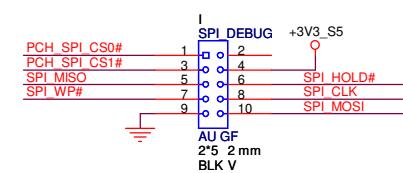
C481 close to U65

ROM1

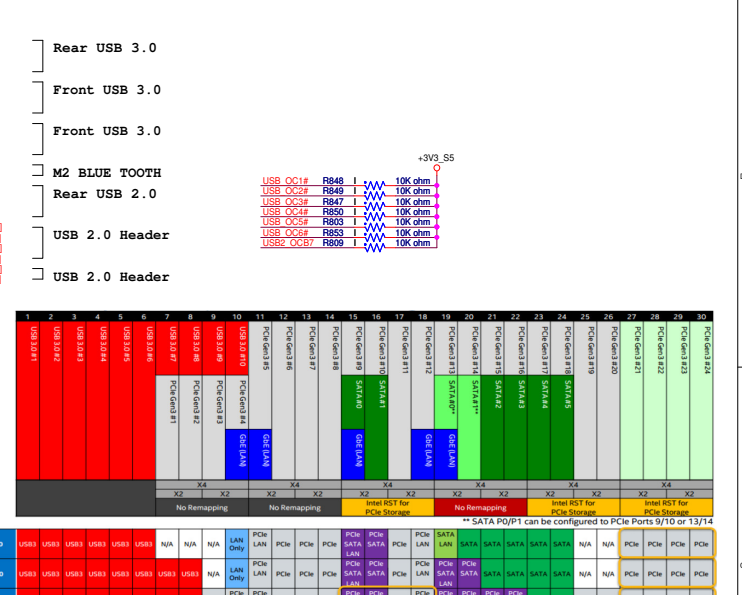
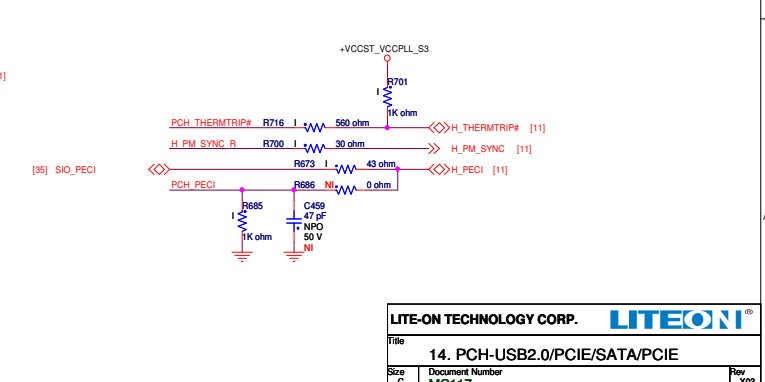
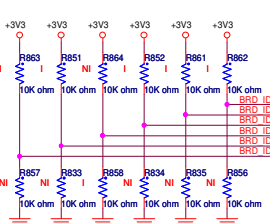


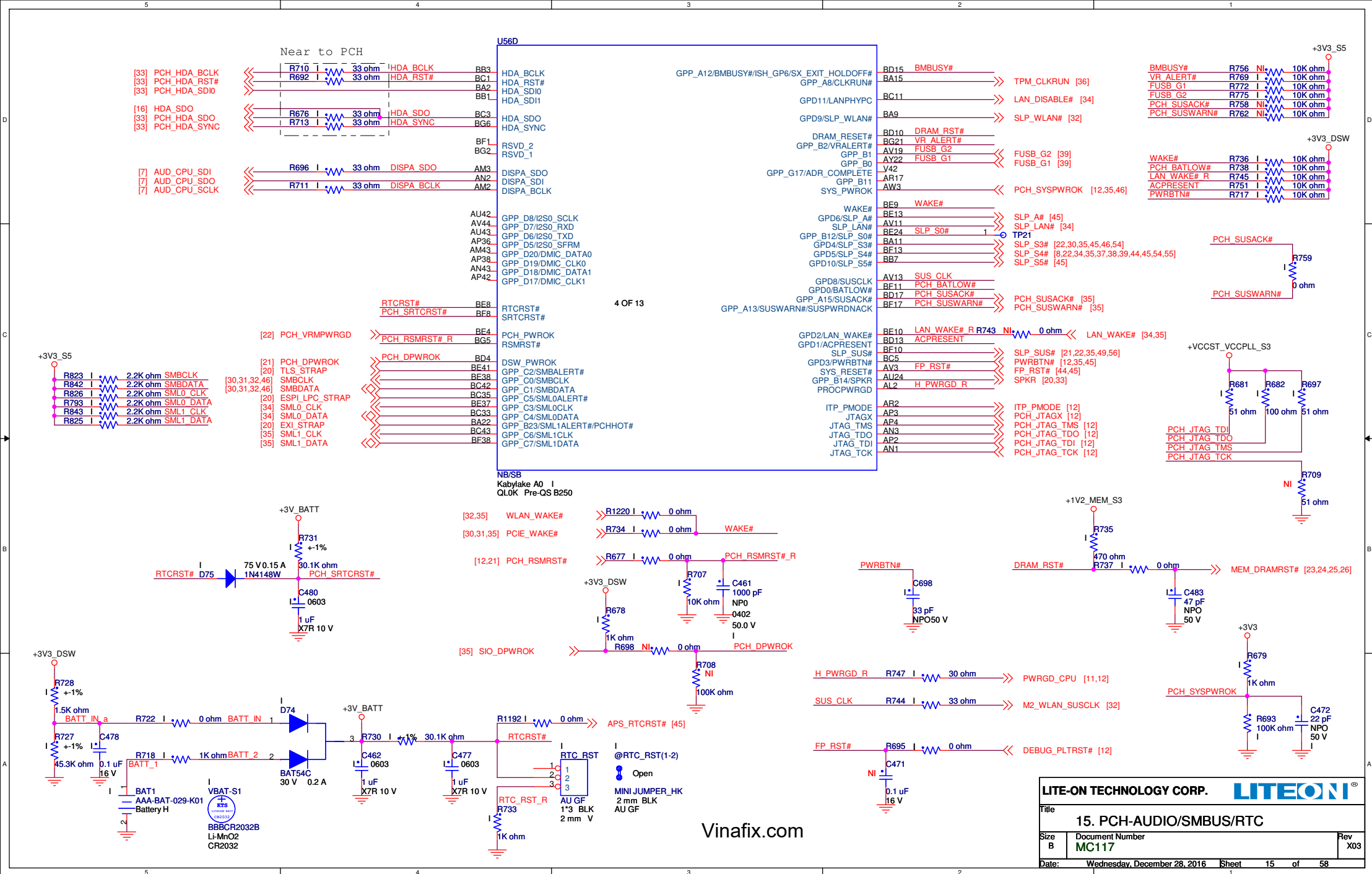
C488 close to U63

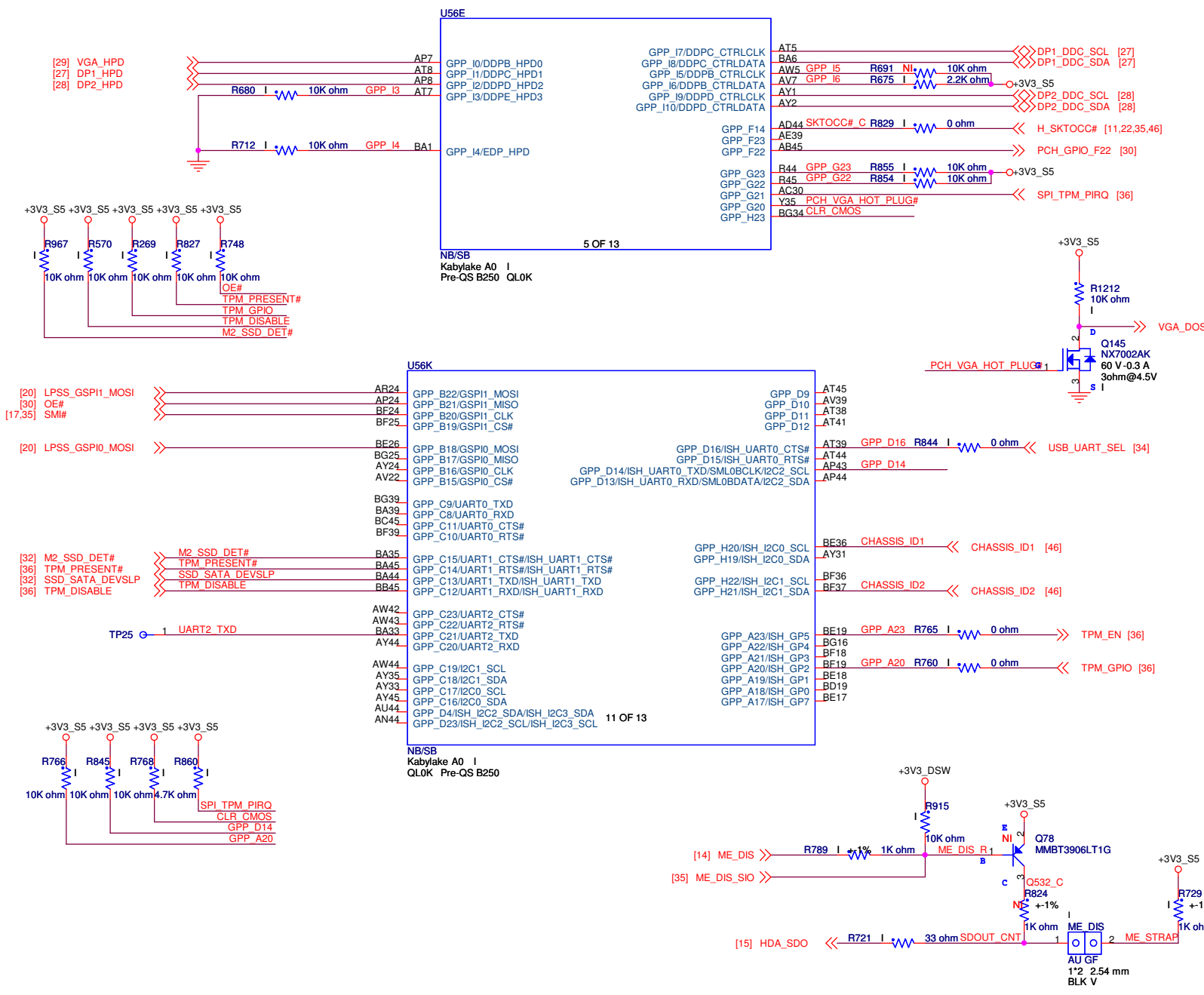
SPI DEBUG



LITE-ON TECHNOLOGY CORP. LITEON®			
Title			
13. PCH-SPI/GPIO			
Size	Document Number	Rev	
B	MC117	X03	
Date:	Wednesday, December 28, 2016	Sheet	13 of 58

[illegible]

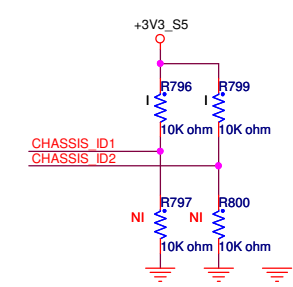
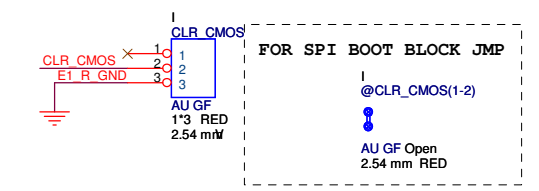




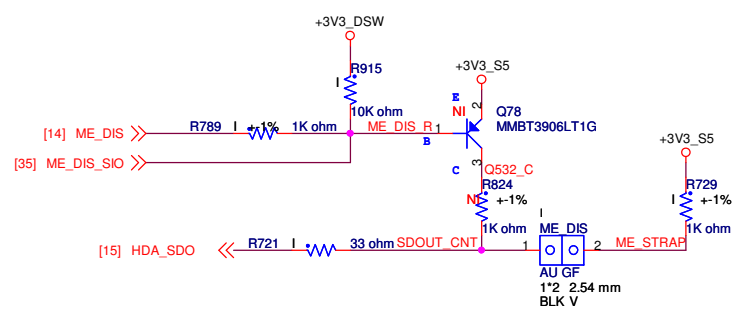
CLEAR CMOS



Jumper	Type
1-2	Default
2-3	CLR_CMOS



Chassis Type	CHASSIS_ID1	CHASSIS_ID2	CHASSIS_ID3
8.5L	L	L	L
15L	H	L	L
18L	L	L	L
TBD(Default)	H	H	H

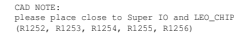


LITE-ON TECHNOLOGY CORP. LITEON®

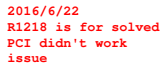
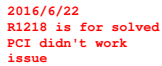
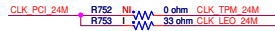
Title16. PCH-GPIO


Size BDocument NumberMC117Rev X03

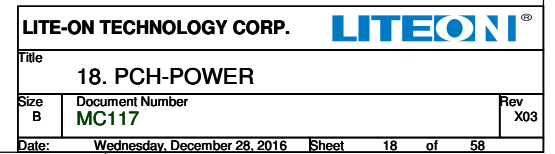
Date: Wednesday, December 28, 2016Sheet 16 of 58



U55 pin8 internal pull high => R705 NI



LITE-ON TECHNOLOGY CORP. 	
Title 17. PCH-USB3/LPC/CLK	
Size C	Document Number MC117
Rev X03	
Date: Wednesday, December 28, 2016 Sheet 17 of 58	





U56I			
A25	VSS_1	VSS_299	A42
A30	VSS_4	VSS_300	D45
P22	VSS_297	VSS_301	BG44
AV38	VSS_157	VSS_302	BF44
AV45	VSS_159	VSS_303	BF45
AV8	VSS_161	VSS_304	BF2
AY11	VSS_163	VSS_305	W29
AY19	VSS_165	VSS_7	A35
AY37	VSS_167	VSS_10	A40
AY4	VSS_169	VSS_13	A41
AY42	VSS_171	VSS_16	AA17
AY8	VSS_173	VSS_19	AA18
B25	VSS_175	VSS_22	AA20
B3	VSS_177	VSS_25	AA21
B30	VSS_179	VSS_28	AA26
B35	VSS_180	VSS_31	AA28
B4	VSS_182	VSS_34	AA29
B41	VSS_184	VSS_37	AB17
BA13	VSS_186	VSS_40	AC32
BA17	VSS_188	VSS_43	AE4
BA29	VSS_190	VSS_46	AE8
BA31	VSS_192	VSS_49	AF18
BA37	VSS_194	VSS_51	AF20
BA4	VSS_196	VSS_53	AF21
BA42	VSS_198	VSS_55	AF25
BB40	VSS_200	VSS_57	AF28
BC38	VSS_202	VSS_59	AF29
BC40	VSS_204	VSS_61	AF4
BC9	VSS_206	VSS_63	AF42
BD11	VSS_208	VSS_65	AG18
BD16	VSS_210	VSS_67	AG20
BD2	VSS_212	VSS_69	AG21
BD21	VSS_214	VSS_71	AG23
BD25	VSS_216	VSS_73	AG25
F2	VSS_218	VSS_75	AG26
E31	VSS_220	VSS_77	AG28
F6	VSS_222	VSS_79	AG29
F8	VSS_224	VSS_81	AH11
F39	VSS_226	VSS_83	AH13
F43	VSS_228	VSS_85	AH30
G4	VSS_230	VSS_87	AH32
G40	VSS_232	VSS_89	AH33
G42	VSS_234	VSS_91	AH38
F6	VSS_236	VSS_93	AJ1
G9	VSS_238	VSS_95	AJ17
H11	VSS_240	VSS_97	AJ18
H13	VSS_242	VSS_99	AJ20
H17	VSS_244	VSS_101	AJ21
H19	VSS_246	VSS_103	AJ23
H22	VSS_248	VSS_105	AJ25
H24	VSS_250	VSS_107	AJ26
H27	VSS_252	VSS_109	AJ28
H29	VSS_254	VSS_111	AJ29
H33	VSS_256	VSS_113	AJ45
H35	VSS_258	VSS_115	AK10
H38	VSS_260	VSS_117	AK14
H4	VSS_262	VSS_119	AK16
H42	VSS_264	VSS_121	AK17
H9	VSS_266	VSS_123	AK18
J4	VSS_268	VSS_125	AK26
M36	VSS_270	VSS_127	AK28
M38	VSS_272	VSS_129	AM14
M4	VSS_274	VSS_131	AN14
M8	VSS_276	VSS_133	AP19
M9	VSS_278	VSS_135	AR22
N13	VSS_280	VSS_137	AR27
N15	VSS_282	VSS_139	AU29
N19	VSS_284	VSS_141	AU33
N22	VSS_286	VSS_143	AV1
N24	VSS_288	VSS_145	AV10
N31	VSS_289	VSS_147	AV15
N42	VSS_291	VSS_149	AV24
P10	VSS_293	VSS_151	AV27
P12	VSS_295	VSS_153	AV33
AV35	VSS_155		

NB/SB
Kabylake A0 I
QL0K Pre-QS B250

9 OF 13

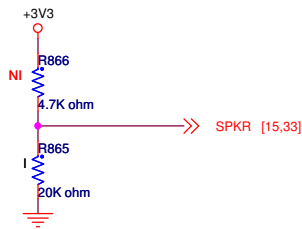
U56L			
BD34	VSS_156	VSS_3	AB18
BD39	VSS_158	VSS_6	AB20
BD7	VSS_160	VSS_9	AB21
BF2	VSS_162	VSS_12	AB25
BF43	VSS_164	VSS_15	AB29
BF5	VSS_166	VSS_18	AB4
BG18	VSS_168	VSS_21	AB42
BG23	VSS_170	VSS_24	AC10
BG28	VSS_172	VSS_27	AC11
BG32	VSS_174	VSS_30	AC14
BG37	VSS_176	VSS_33	AC16
BG40	VSS_178	VSS_36	AC38
BG9	VSS_181	VSS_39	AC4
C1	VSS_183	VSS_42	AC5
A12	VSS_185	VSS_45	AC7
C2	VSS_187	VSS_48	AC8
C37	VSS_189	VSS_50	AD1
A6	VSS_191	VSS_52	AD18
C9	VSS_193	VSS_54	AD20
D1	VSS_195	VSS_56	AD21
D10	VSS_197	VSS_58	AD25
D12	VSS_199	VSS_60	AD29
D15	VSS_201	VSS_62	AD45
D16	VSS_203	VSS_64	AE11
B12	VSS_205	VSS_66	AE14
D19	VSS_207	VSS_68	AE32
D21	VSS_209	VSS_70	AE33
D24	VSS_211	VSS_72	AE38
D25	VSS_213	VSS_74	AK29
D29	VSS_215	VSS_76	AK30
D30	VSS_217	VSS_78	AK32
D33	VSS_219	VSS_80	AK35
D35	VSS_221	VSS_82	AK39
D36	VSS_223	VSS_84	AL4
D39	VSS_225	VSS_86	AL42
D44	VSS_227	VSS_88	AM10
D7	VSS_229	VSS_90	AM11
P13	VSS_231	VSS_92	AM13
P15	VSS_233	VSS_94	AM17
P17	VSS_235	VSS_96	AM19
P19	VSS_237	VSS_98	AM24
P31	VSS_239	VSS_100	AM27
P33	VSS_241	VSS_102	AM29
P35	VSS_243	VSS_104	AM32
P4	VSS_245	VSS_106	AM33
P42	VSS_247	VSS_108	AM4
P8	VSS_249	VSS_110	AN45
R1	VSS_251	VSS_112	AP10
R32	VSS_253	VSS_114	AP11
T10	VSS_255	VSS_116	AP13
T14	VSS_257	VSS_118	AP15
T22	VSS_259	VSS_120	AP22
T29	VSS_261	VSS_122	AP27
T32	VSS_263	VSS_124	AP31
T36	VSS_265	VSS_126	AP33
T38	VSS_267	VSS_128	AP34
Y38	VSS_269	VSS_130	AP39
Y4	VSS_271	VSS_132	T4
Y8	VSS_273	VSS_134	W26
T42	VSS_275	VSS_136	V16
T5	VSS_277	VSS_138	V17
U4	VSS_279	VSS_140	V18
U42	VSS_281	VSS_142	V30
V10	VSS_283	VSS_144	V32
V14	VSS_285	VSS_146	V33
W3	VSS_287	VSS_148	V38
AR13	VSS_289	VSS_150	V4
AR31	VSS_291	VSS_152	V8
AR33	VSS_293	VSS_154	W18
AR4	VSS_295	VSS_156	W20
AT10	VSS_297	VSS_158	W21
AT13	VSS_299	VSS_160	W23
AT35	VSS_301	VSS_162	W25
AT37	VSS_303	VSS_164	
AT42	VSS_305	VSS_166	
AU11	VSS_307	VSS_168	A44
AU17	VSS_309	VSS_170	BE1
BD30	VSS_311	VSS_172	BD1
W45	VSS_313	VSS_174	B1
Y13	VSS_315	VSS_176	A2
Y14	VSS_317	VSS_178	B2
Y30	VSS_319	VSS_180	A3
Y32	VSS_321	VSS_182	A4
Y33	VSS_323	VSS_184	B44
BG14	VSS_325	VSS_186	B45
	VSS_327	VSS_188	
	VSS_329	VSS_190	
	VSS_331	VSS_192	
	VSS_333	VSS_194	

NB/SB
Kabylake A0 I
QL0K Pre-QS B250

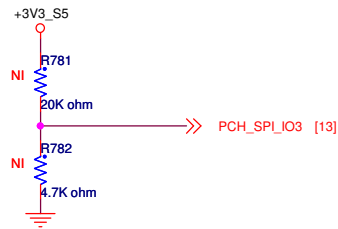
12 OF 13

LITE-ON TECHNOLOGY CORP.		LITEON®	
Title			
19. PCH-VSS			
Size	Document Number	Rev	
B	MC117	X03	
Date:	Wednesday, December 28, 2016	Sheet	19 of 58

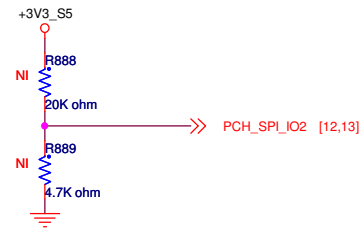
TOP SWAP OVERRIDE STRAP (INTERNAL PD)	
HIGH	ENABLED
LOW	DISABLED (DEFAULT)



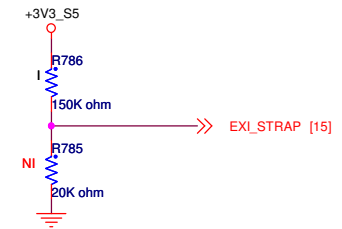
CONSENT STRAP (INTERNAL PU)	
HIGH	DISABLED (DEFAULT)
LOW	ENABLED



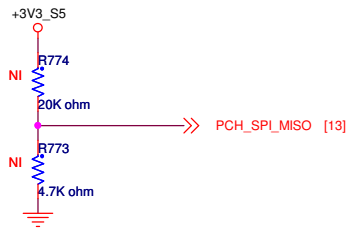
CONSENT STRAP (INTERNAL PU)	
HIGH	DISABLED (DEFAULT)
LOW	ENABLED



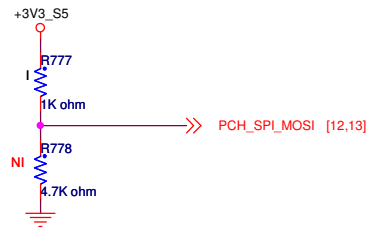
EXI BOOT STALL BYPASS (INTERNAL PD)	
HIGH	ENABLE
LOW	DISABLE (DEFAULT)



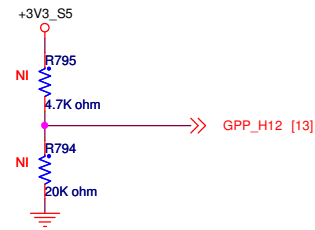
JTAG ODT (INTERNAL PU)	
HIGH	ENABLED (DEFAULT)
LOW	DISABLED



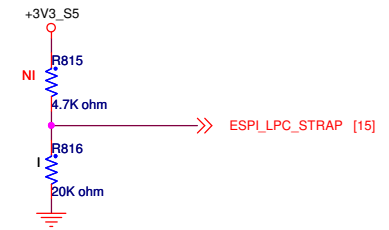
BOOT HALT (INTERNAL PU)	
HIGH	DISABLED (DEFAULT)
LOW	ENABLED



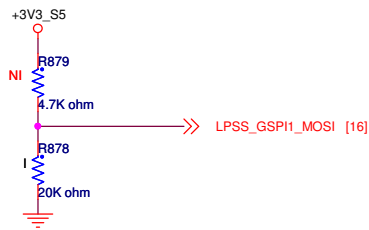
ESPI FLASH SHARING MODE (INTERNAL PD)	
HIGH	SLAVE ATTACHED FLASH SHARING
LOW	MASTER ATTACHED FLASH SHARING



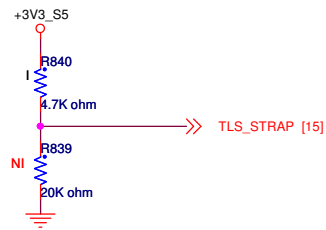
ESPI/LPC SELECT (INTERNAL PD)	
HIGH	ESPI
LOW	LPC



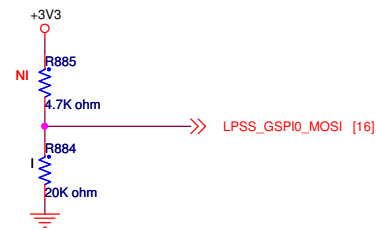
BOOT SELECT (INTERNAL PD)	
HIGH	LPC
LOW	SPI (DEFAULT)



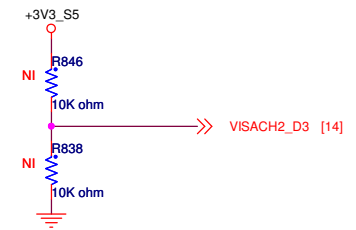
TLS CONFIDENTIALITY (INTERNAL PD)	
HIGH	ENABLED (DEFAULT)
LOW	DISABLED



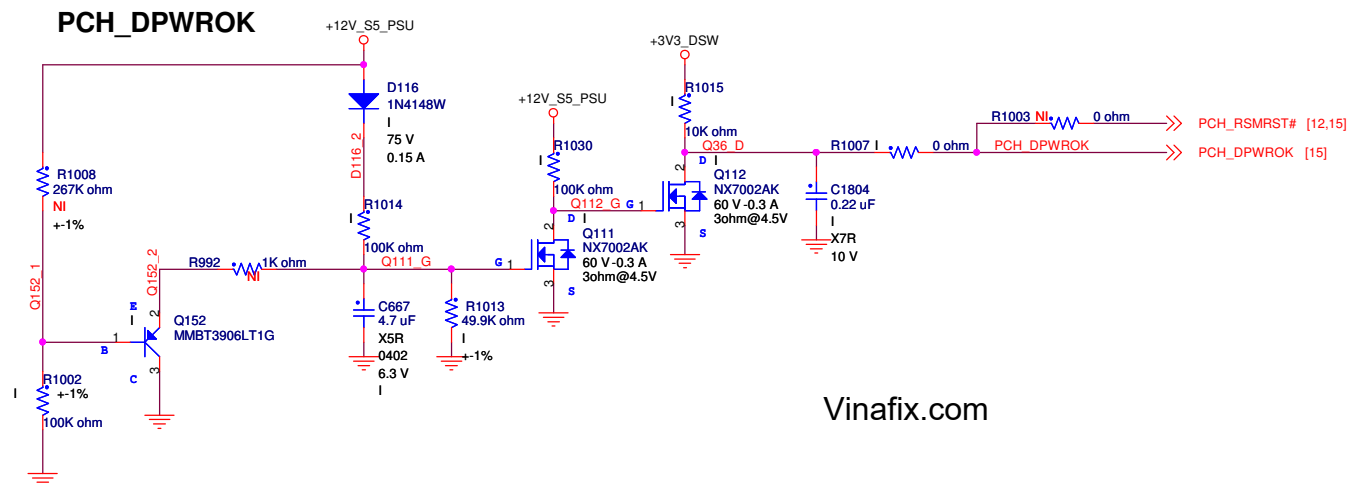
REBOOT (INTERNAL PD)	
HIGH	NO REBOOT
LOW	REBOOT (DEFAULT)



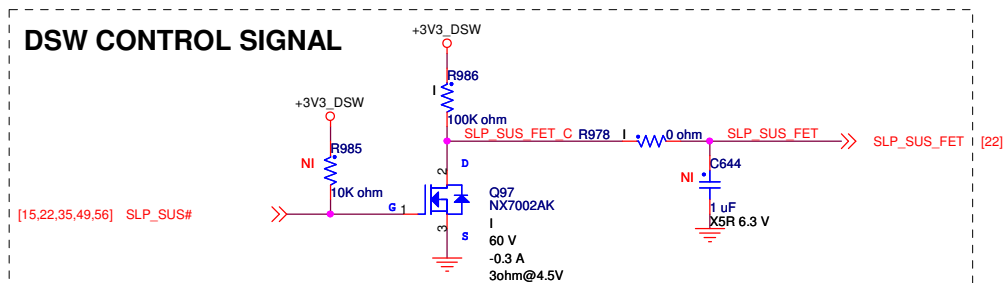
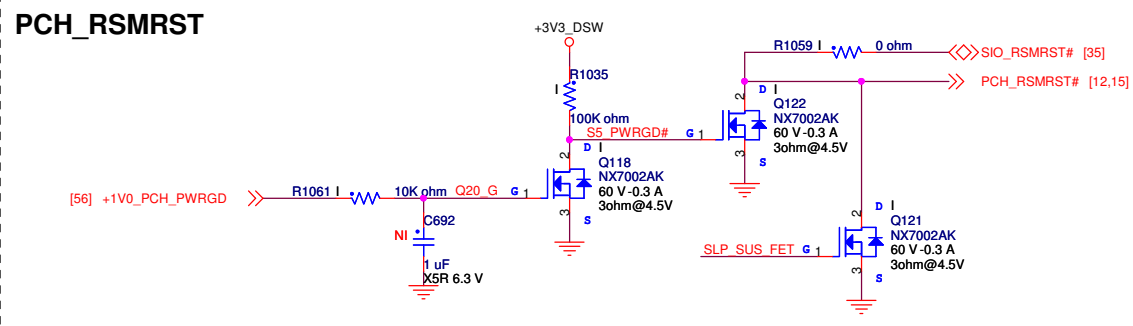
DFX TEST MODE (INTERNAL PD)	
HIGH	XTAL INPUT IS DIFFERENTIAL
LOW	XTAL INPUT IS SINGLE END

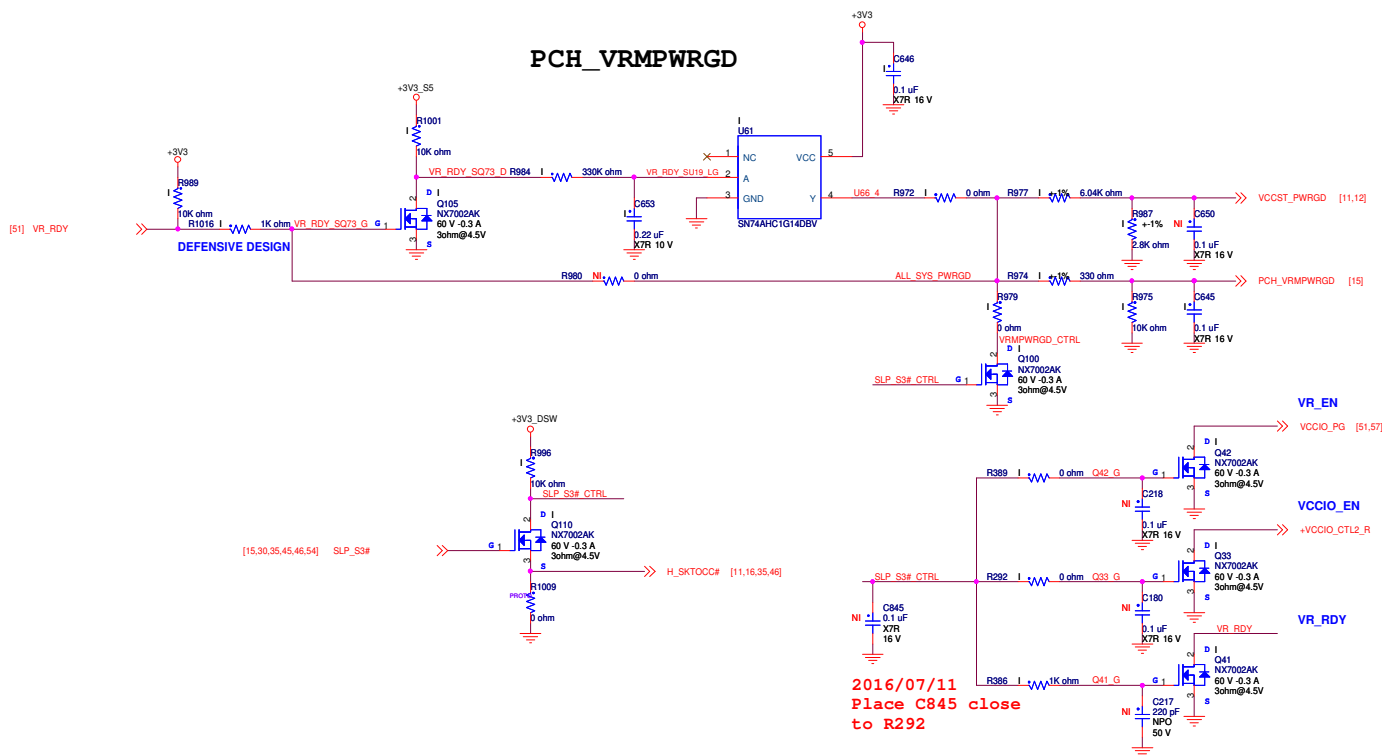


05/20: Change R1030 power source from +5V_S5 to +12V_S5_PSU (Start to modify from X03)
05/20: Rework R1030.1 from +5V_S5 to +12V_S5_PSU (Jump wire)

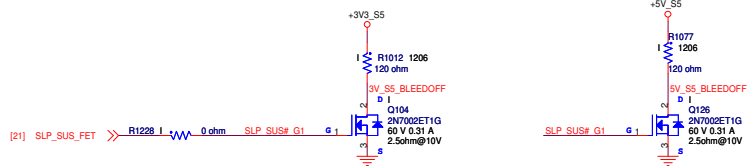


Vinafix.com

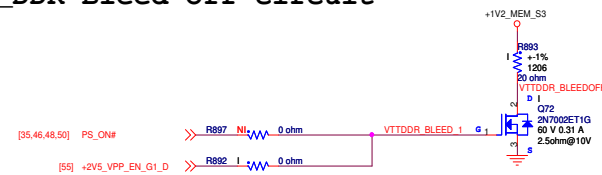




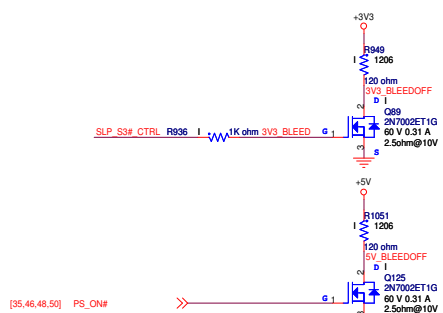
5V_S5 Bleed off circuit



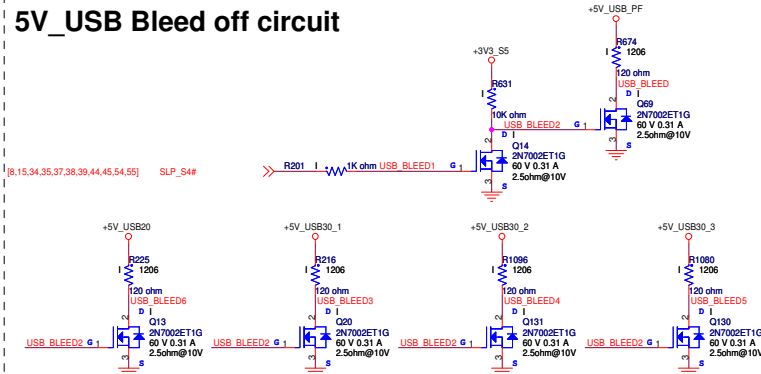
+1V2_DDR Bleed off circuit

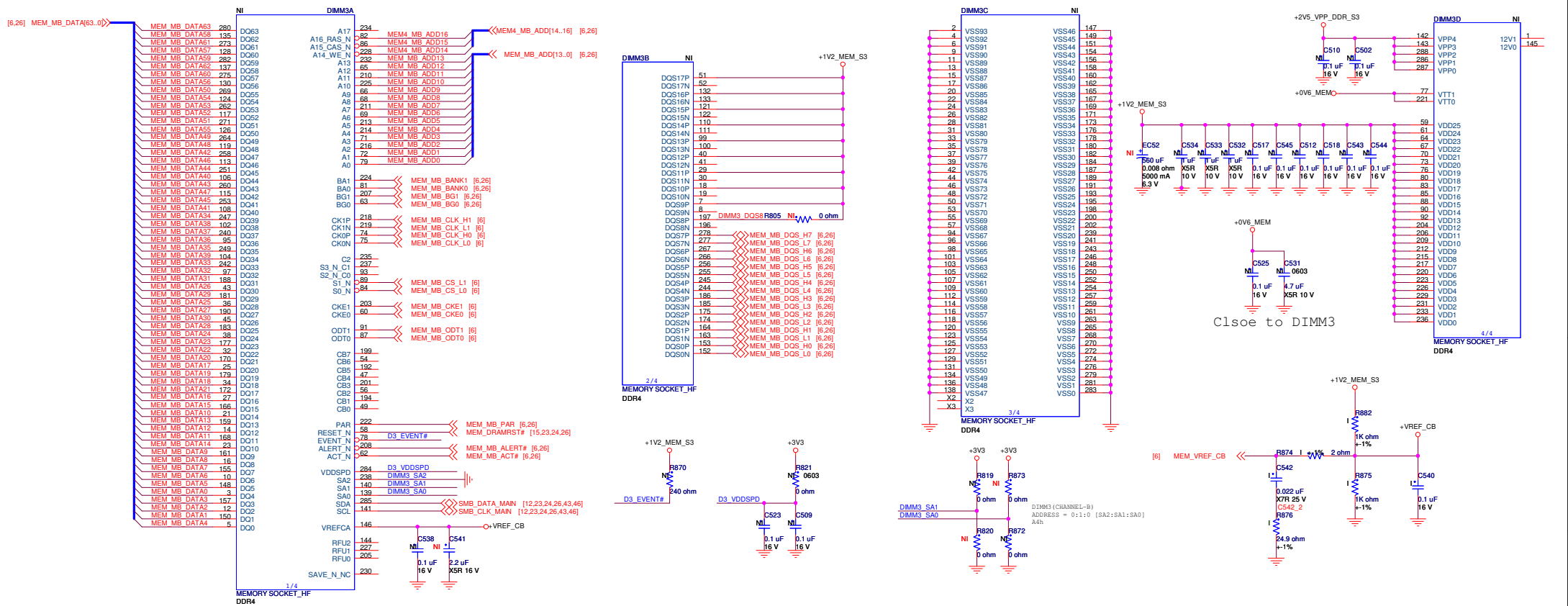


5V & 3.3V Bleed off circuit



5V_USB Bleed off circuit





Vinafix.com

LITE-ON TECHNOLOGY CORP.

LITEON

25. DDR4 CHB UDIMM3

Size Customer Document Number Rev

MC117 X03

Date

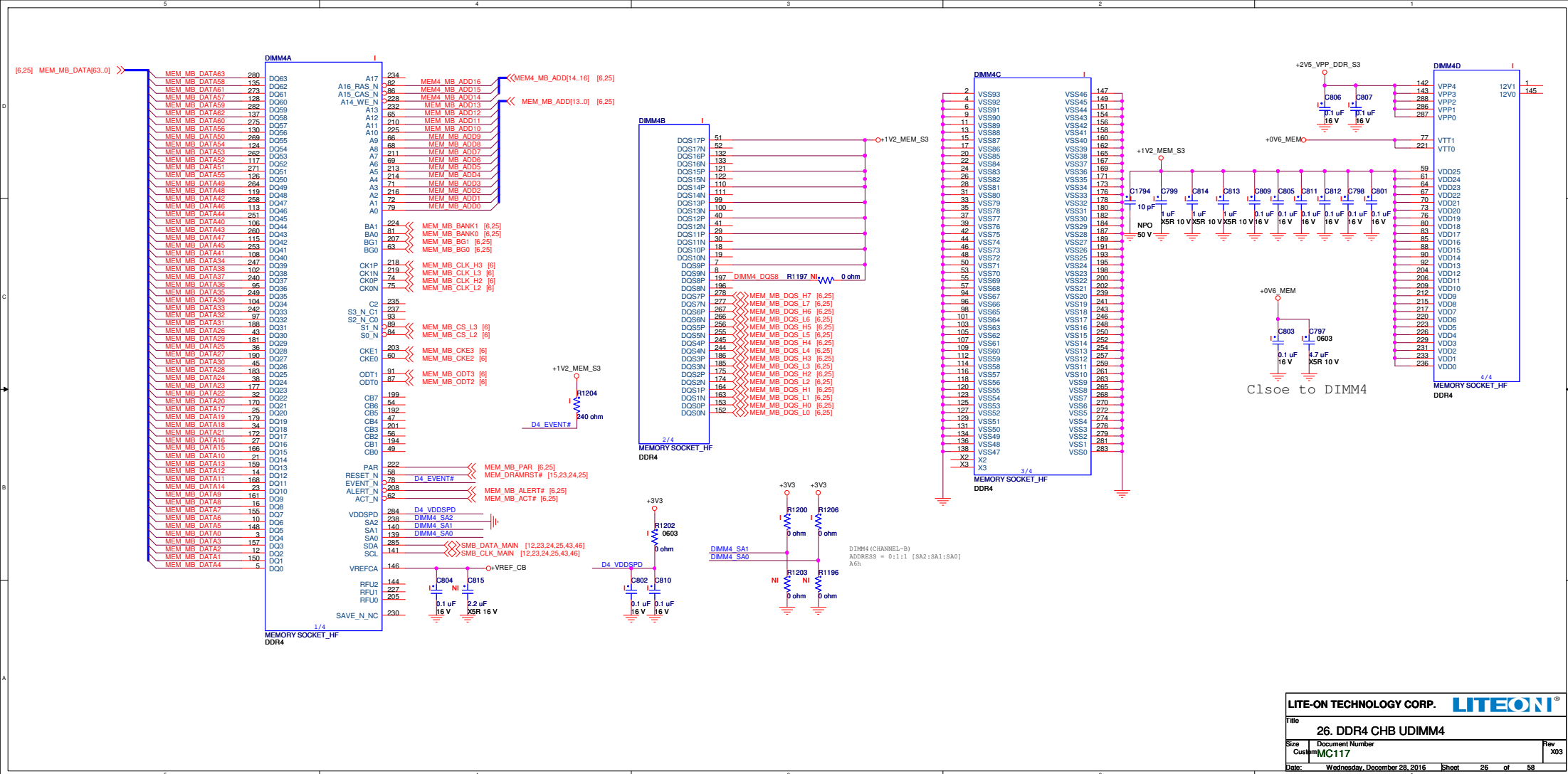
Wednesday, December 28, 2016

Sheet

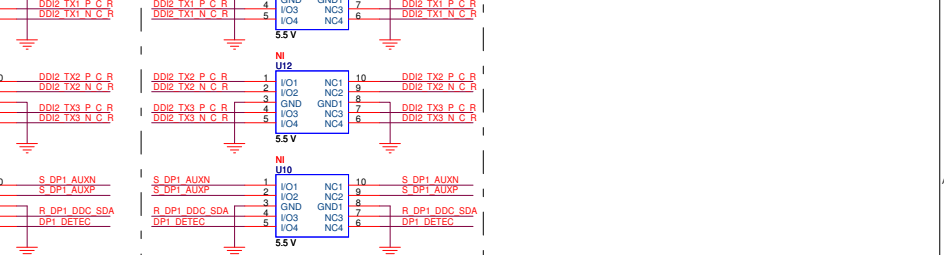
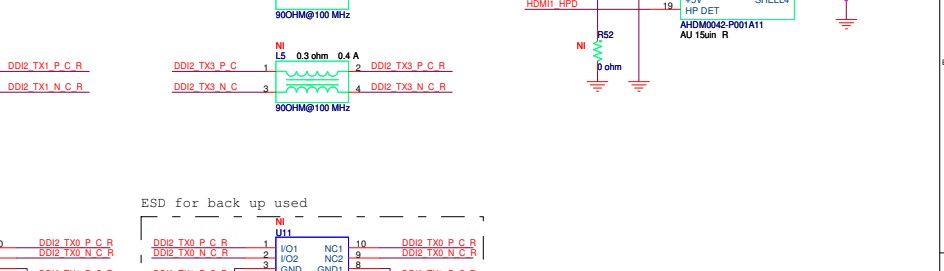
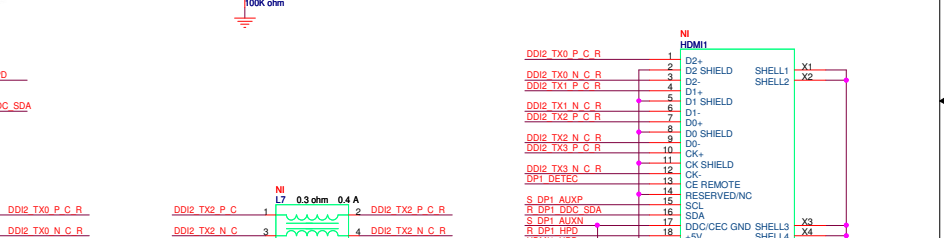
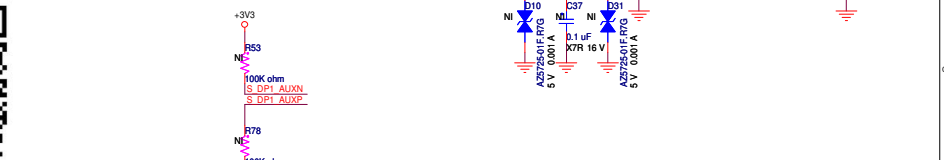
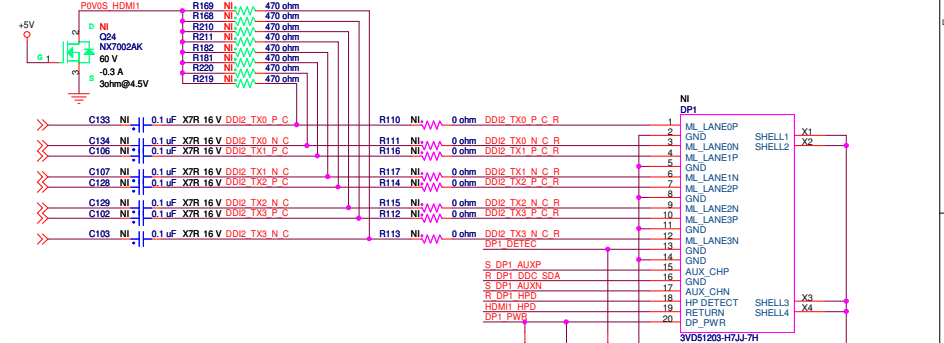
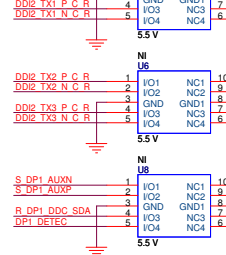
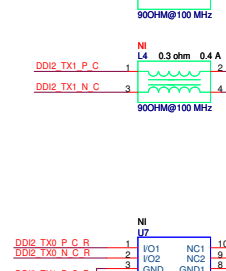
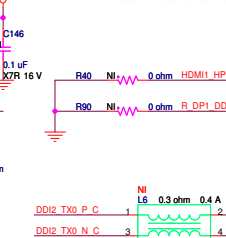
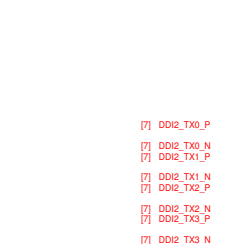
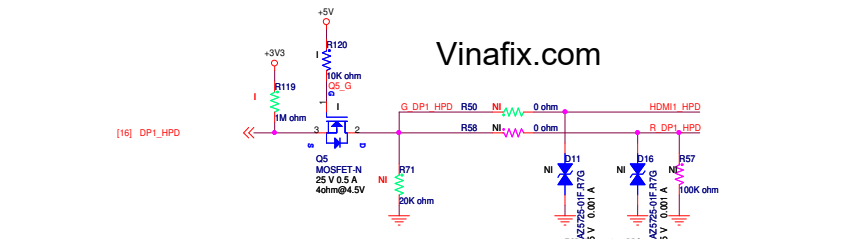
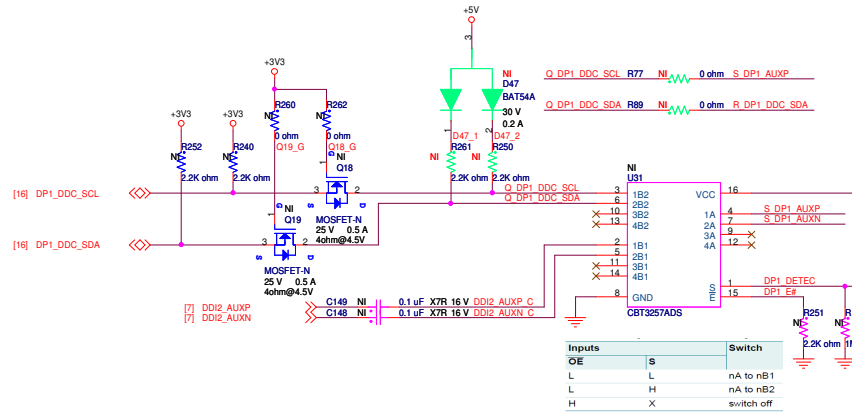
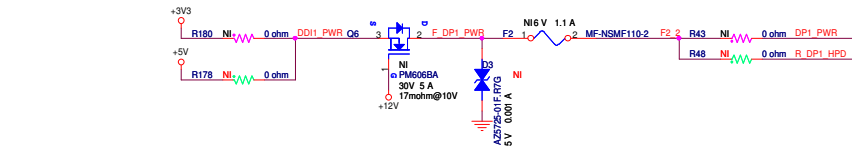
25

of

58

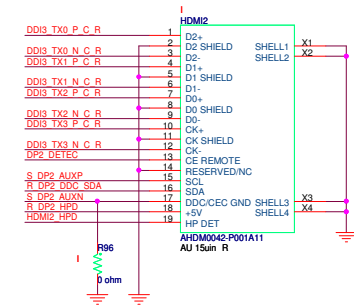
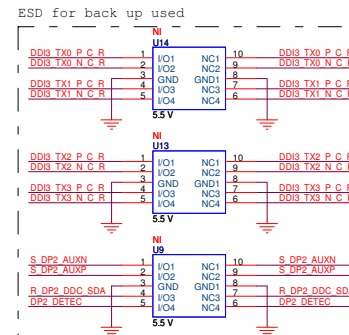
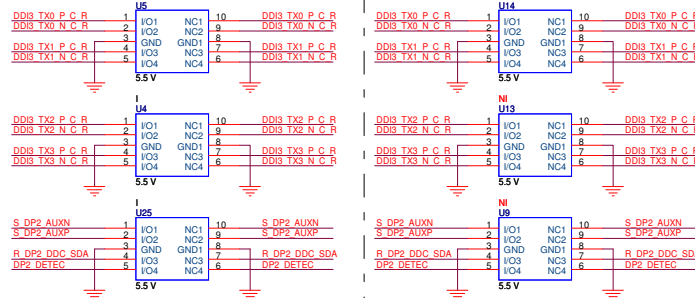
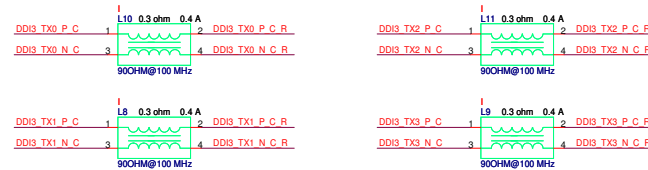
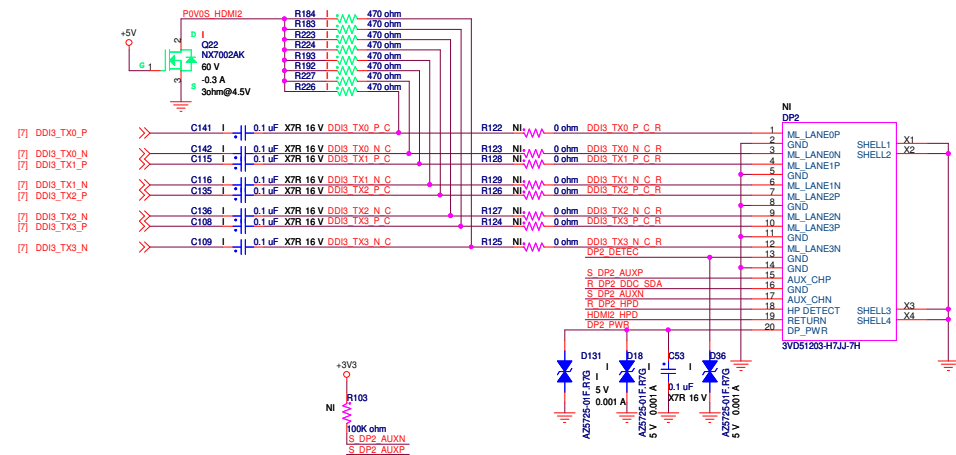
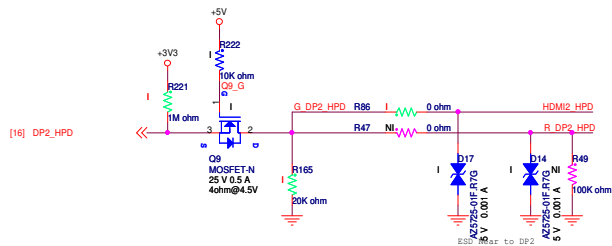
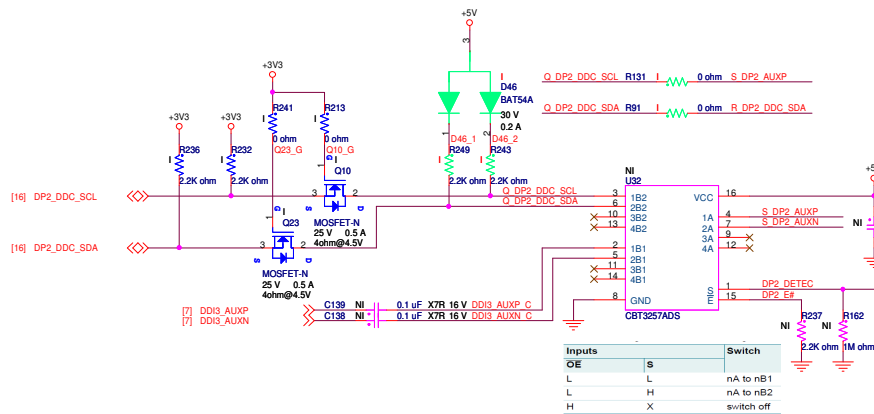
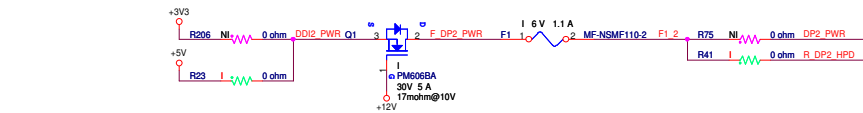


A : DP
B : HDMI

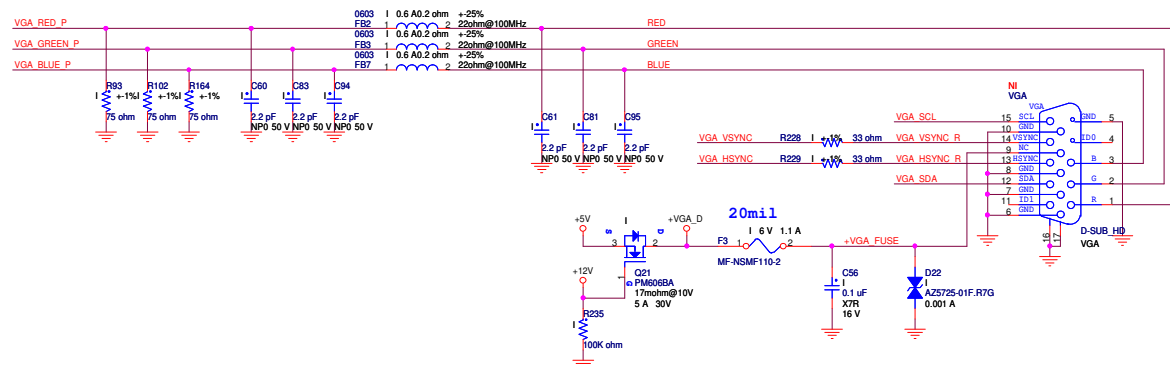
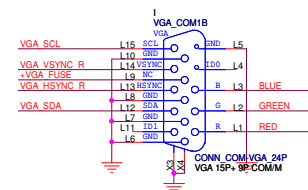
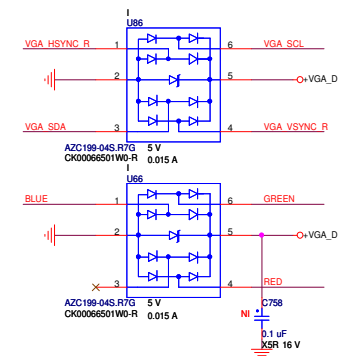
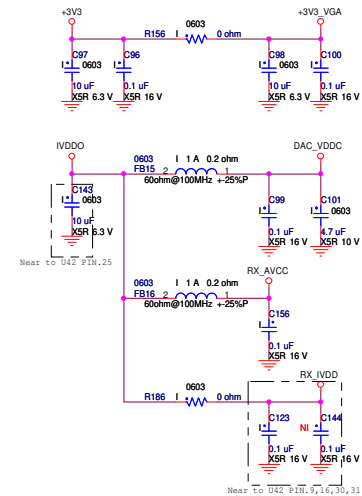
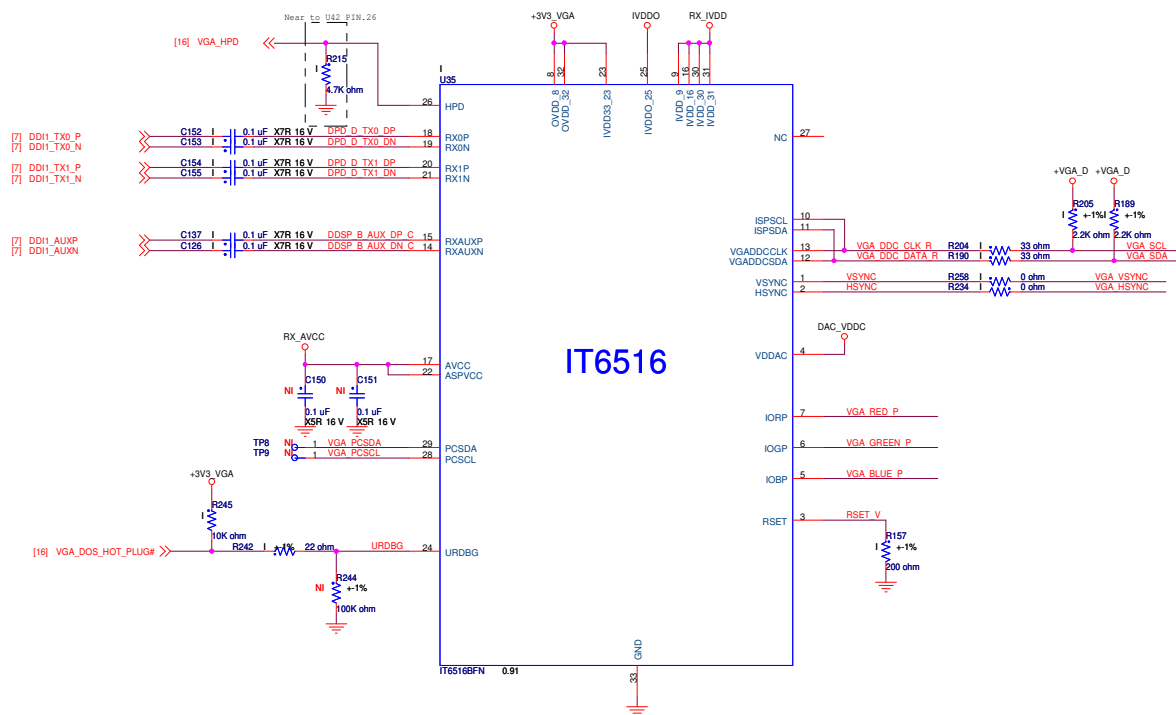


Vinafix.com

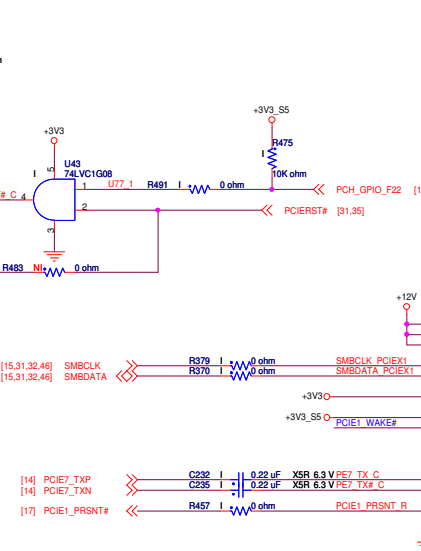
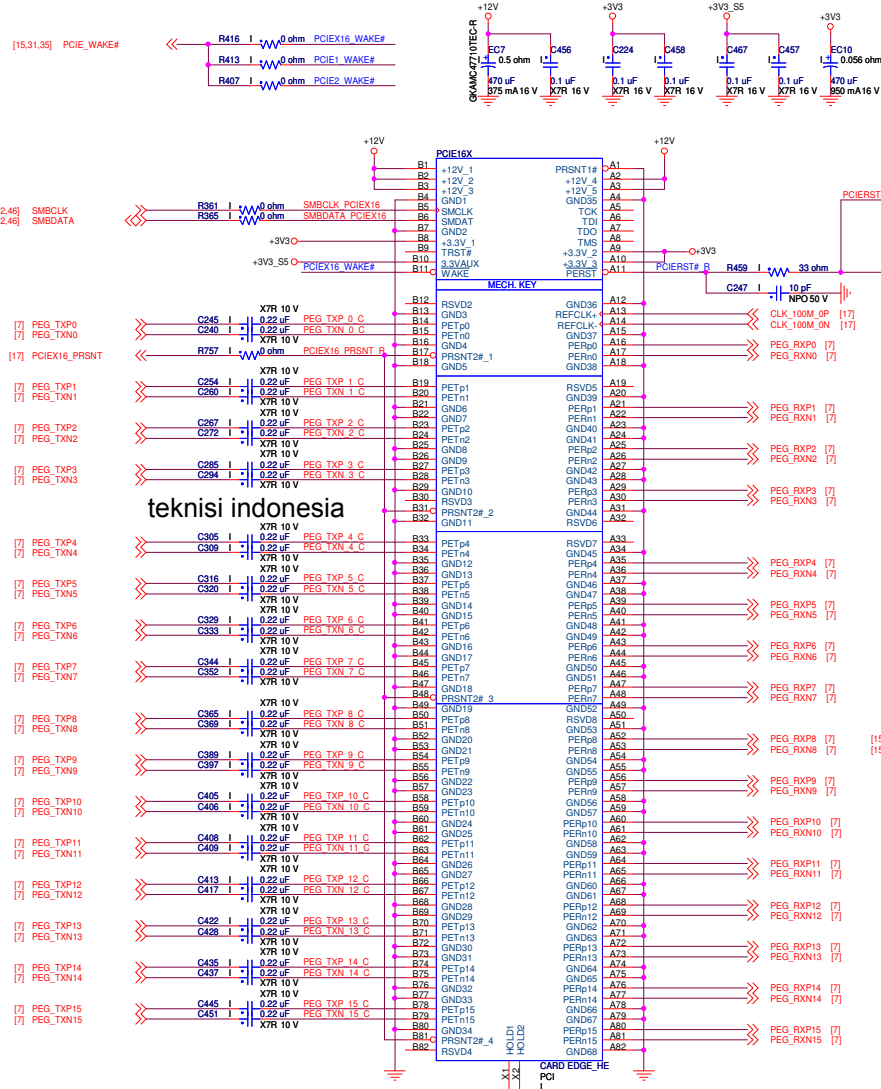
A : DP
B : HDMI



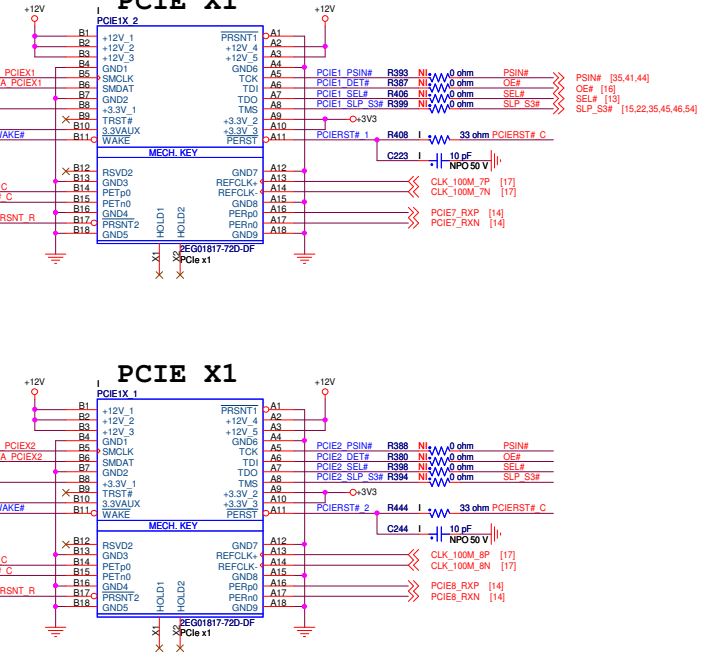
DP to VGA - Bridge IT6516B

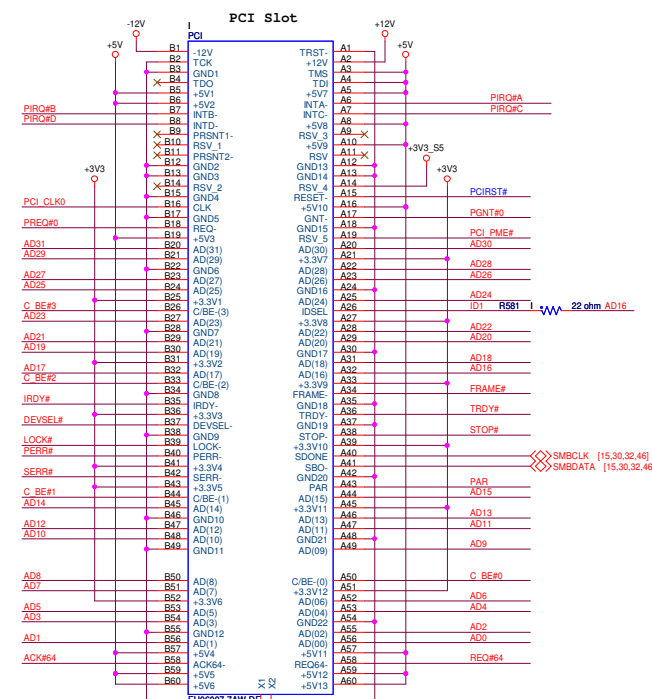
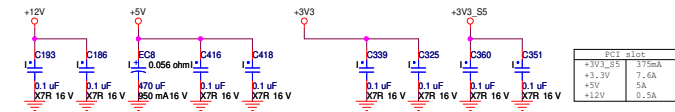
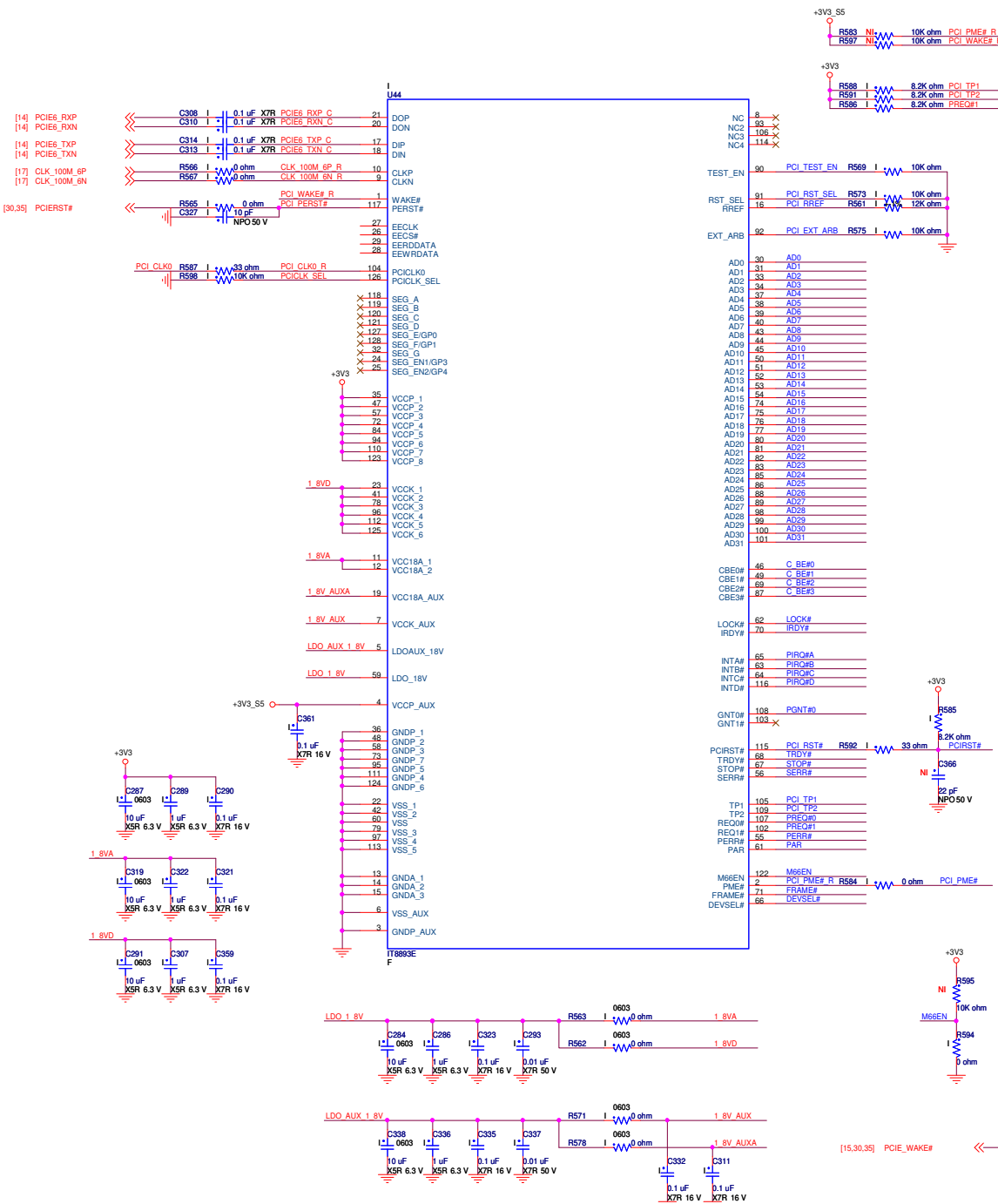


PCIE X16

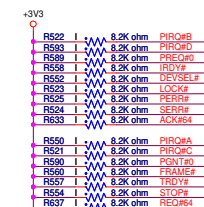


PCIE X1





IDESEL = AD16
MASTER = PREQ#0
PIRQ#A



Vinafix.com

STANDOFF_RQ
M/M M2.0
ROUND
Brass Lead Free



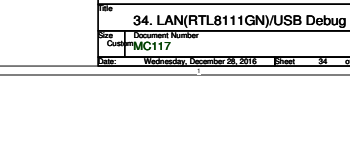
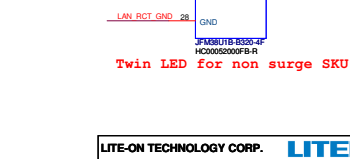
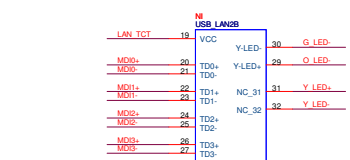
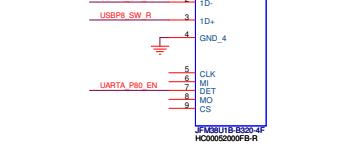
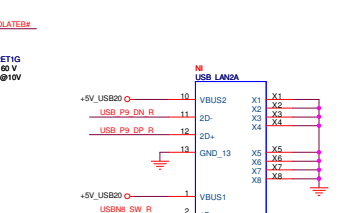
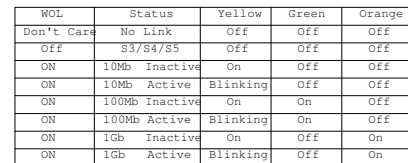
The schematic diagram illustrates the M2 SSD connection for the Raspberry Pi 4B. It is divided into two main sections: the M2 SSD connection and the M2 SSD DET# connection.

M2 SSD Connection:

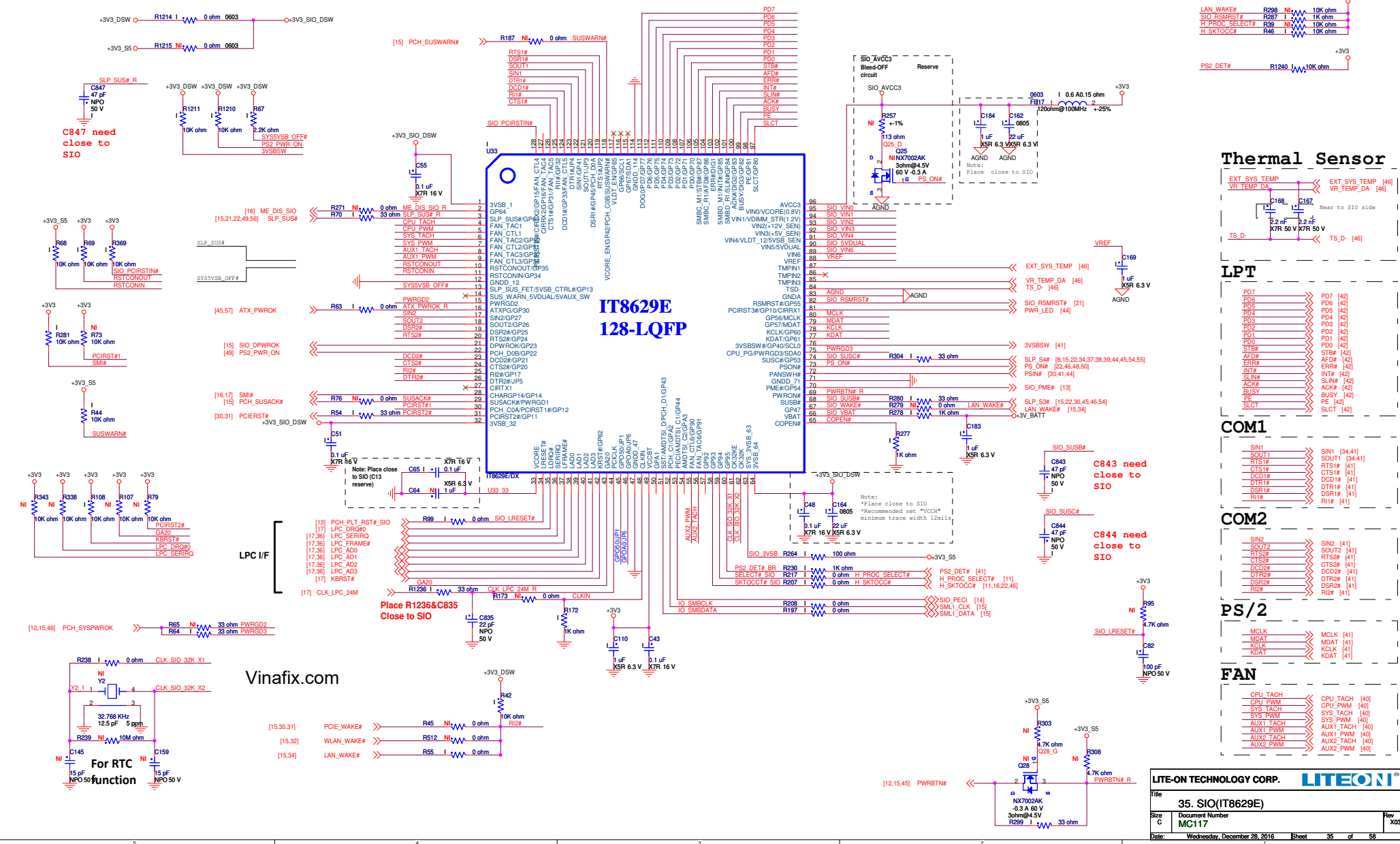
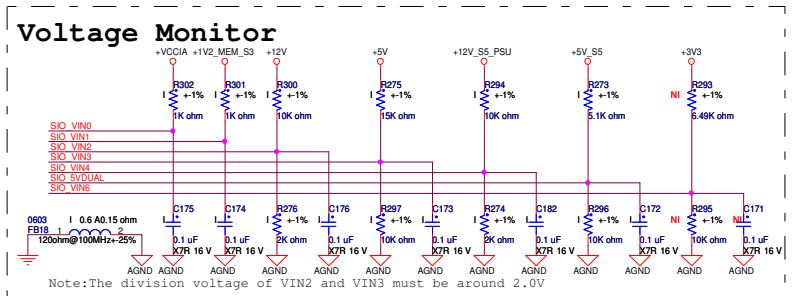
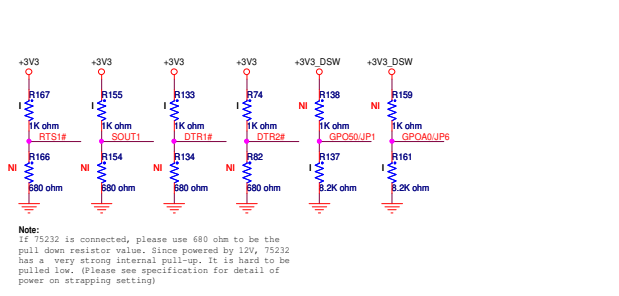
- Left Side (M2 SSD DET#):** Shows the connection of the M2 SSD DET# pin (R964) to the M2 SSD DET# R pin. It includes a 0 ohm resistor (R964) and a 0.22 uF capacitor (C583, C580).
- Right Side (M2 SSD):** Shows the connection of the M2 SSD pins (1-58) to the M2 SSD pins (1-58). It includes various components like resistors (R841, R958, R960), capacitors (C551, C539, C556, C557), and jumpers (J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58).

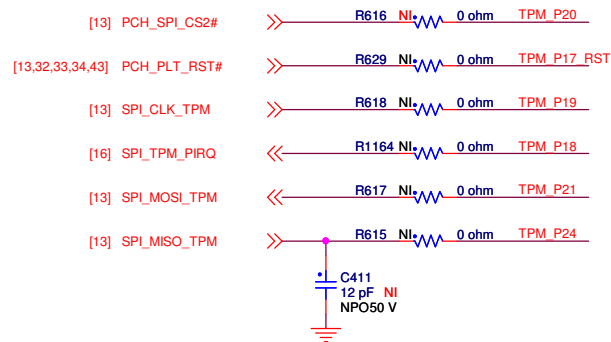
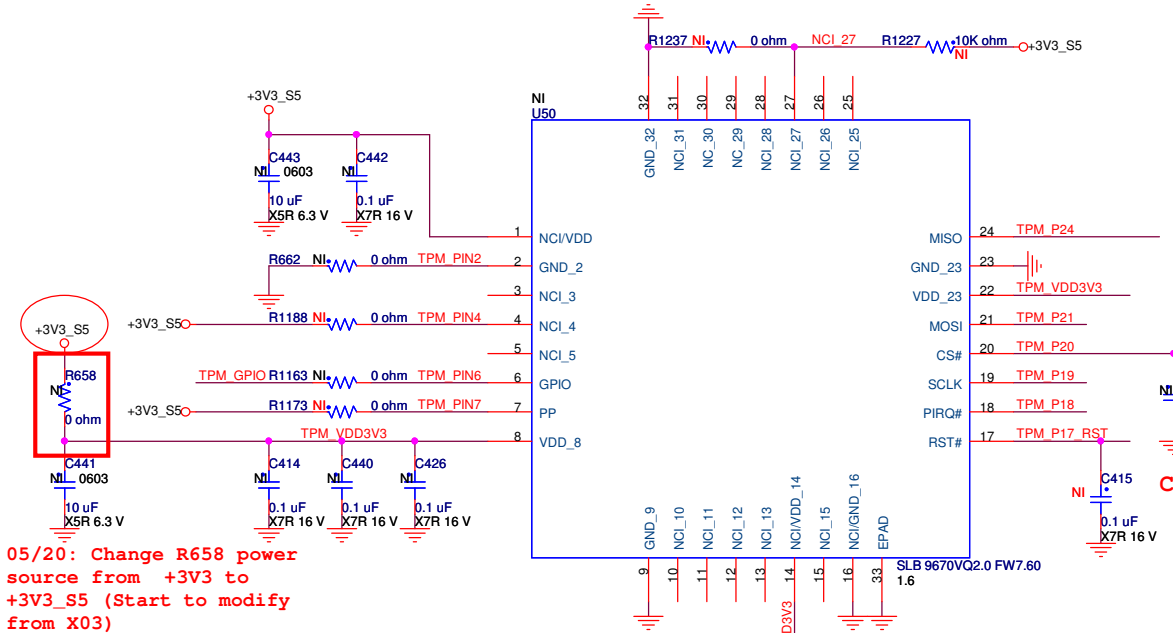
M2 SSD DET# Connection:

- Left Side (M2 SSD DET#):** Shows the connection of the M2 SSD DET# pin (R964) to the M2 SSD DET# R pin. It includes a 0 ohm resistor (R964) and a 0.22 uF capacitor (C583, C580).
- Right Side (M2 SSD DET#):** Shows the connection of the M2 SSD DET# pins (1-58) to the M2 SSD DET# pins (1-58). It includes various components like resistors (R841, R958, R960), capacitors (C551, C539, C556, C557), and jumpers (J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58).



Power-On Strapping			
Symbol	Value	Description	
JP1	DSW_EUP_SEL	1	EUP
Pin-45		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-119		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h/7B/A3/ABh=80h
Pin-121		0	EC Index 63h/6Bh/73h/7B/A3/ABh=00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-123		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-26	OV/UV	0	Force Mode
JP6	Vih/Vil_SEL	1	Bay-Trail Platform (Default)
Pin-46		0	Not Bay-Trail Platform





BOM	PIN	NCT650LBAYX (SPI)	BT00012901IB-R SLB9670 (SPI)	ST33HTPH2E32AAE8 (SPI)
GND	2	NI	R662	R662
NCI_4	4	NI	NI	NI
GPIO	6	NI	R1163	NI
PP	7	NI	NI	NI
IRQ# (R1164) / AD2 (R628)	18	R1164	R1164	R1164
CLK	19	R618	R618	R618
CS# (R616) / LPC Frame# (R625)	20	R616	R616	R616
MOSI (R617) / AD1 (R626)	21	R617	R617	R617
MISO (R615) / AD0 (R624)	24	R615	R615	R615
NCI_27	27	R1227	NI	NI

For Nuvoton TPM , Can remove R1164 and R860 if IRQ function was no used.

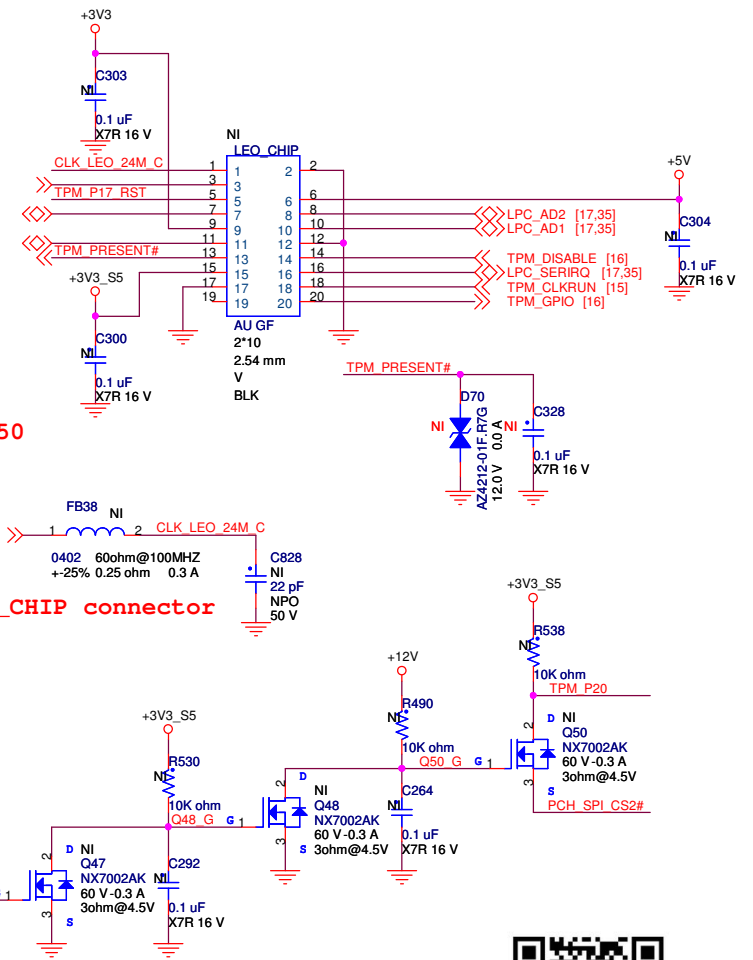
[17,35] LPC_FRAME#
[17,35] LPC_AD3
[17,35] LPC_AD0
[16] TPM_PRESENT#

C842 close to U50

C10se to LEO_CHIP connector

[16] TPM_EN

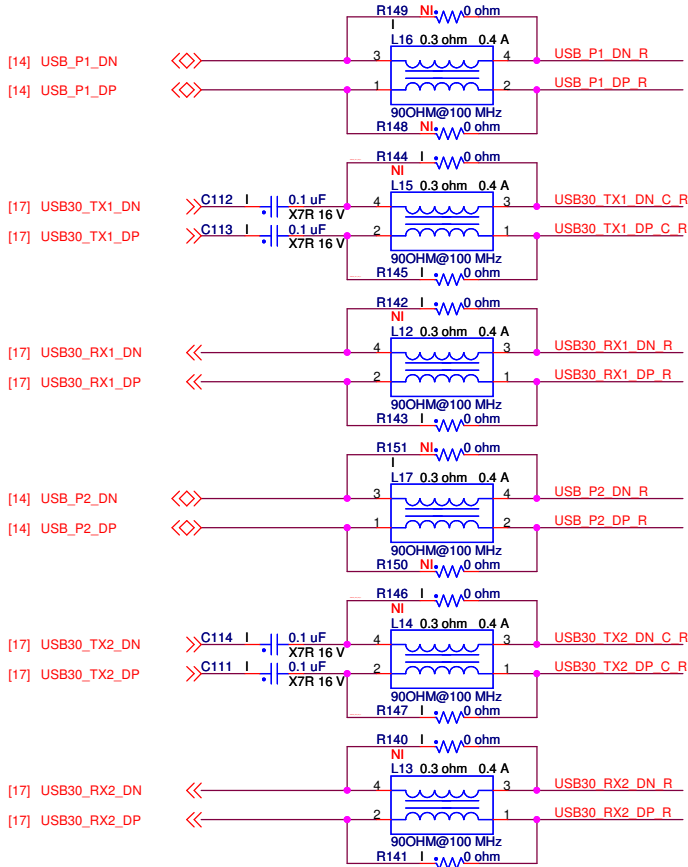
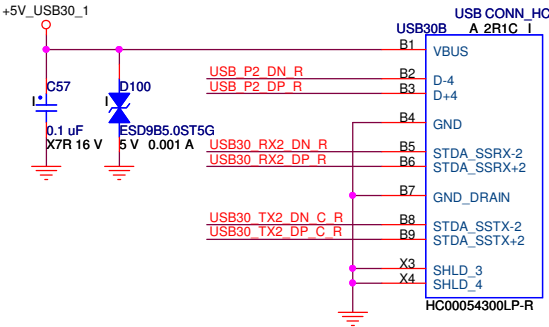
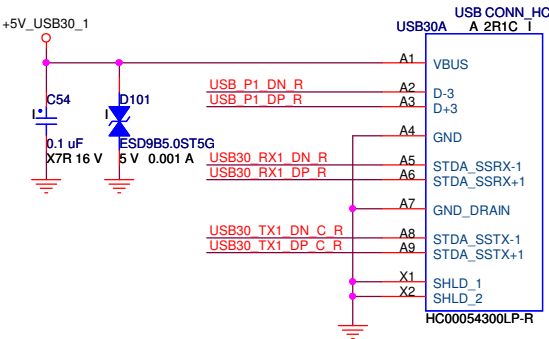
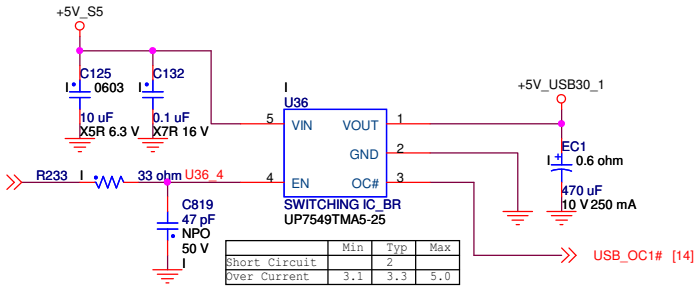
C415 for power on sequence fine tuning
(Nuvoton: That RESET# is asserted for at least 5 msec following the VSB power up and at least 1ms following the VDD power up)



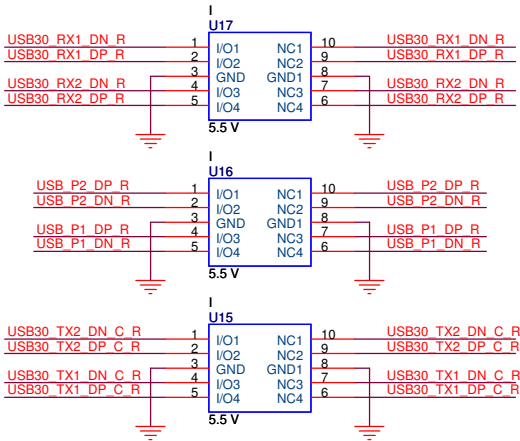
LITE-ON TECHNOLOGY CORP. LITEON®		
Title 36. TPM2.0		
Size B	Document Number MC117	Rev X03
Date:	Wednesday, December 28, 2016	Sheet 36 of 58

Rear USB 3.0

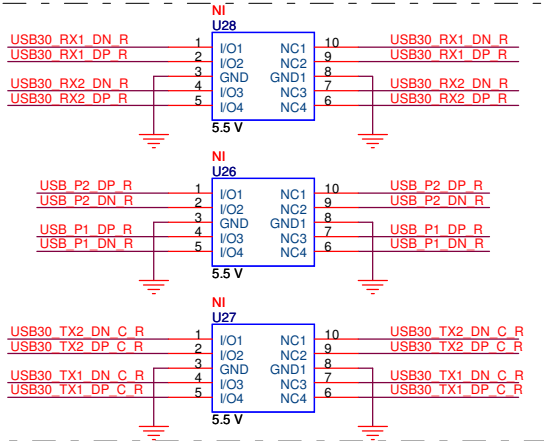
[8,15,22,34,35,38,39,44,45,54,55] SLP_S4#



Vinafix.com

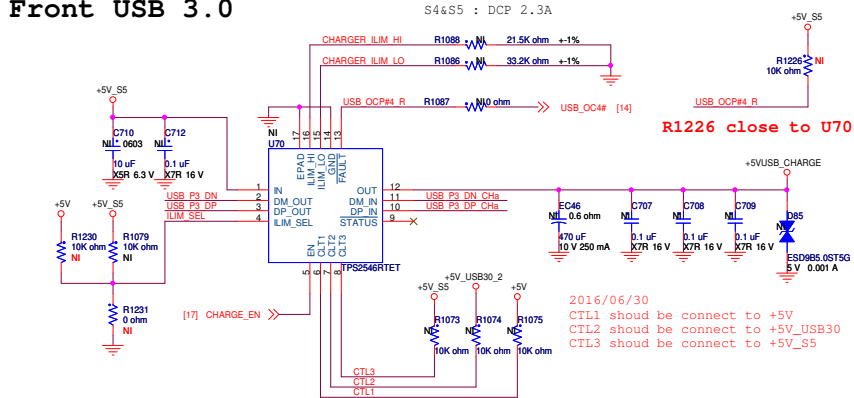


ESD for back up used

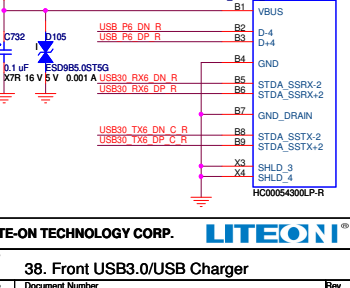
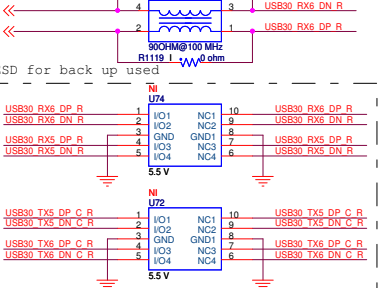
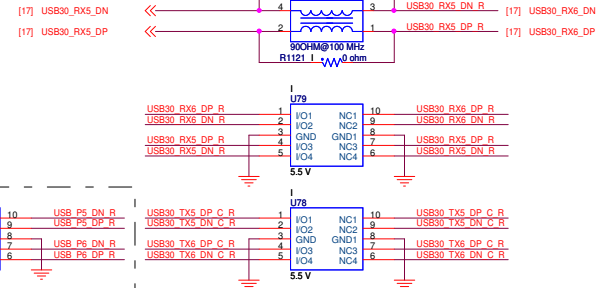
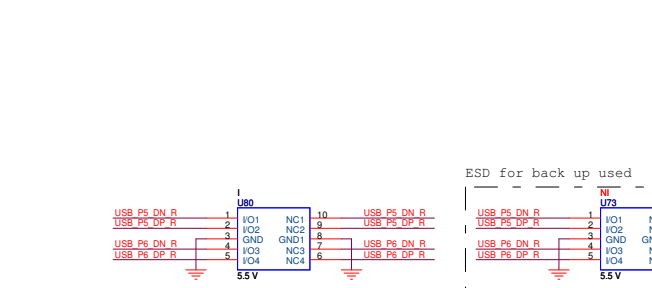
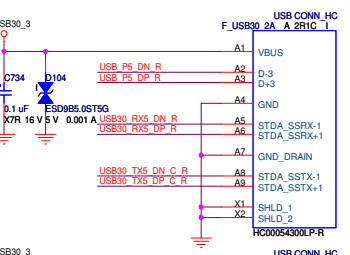
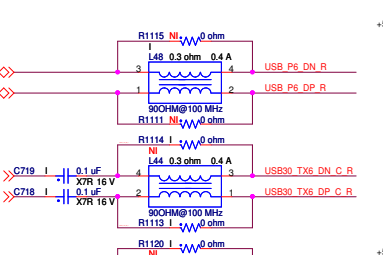
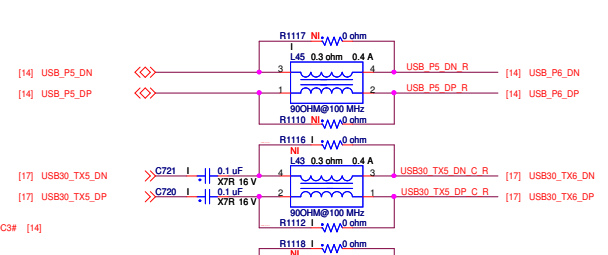
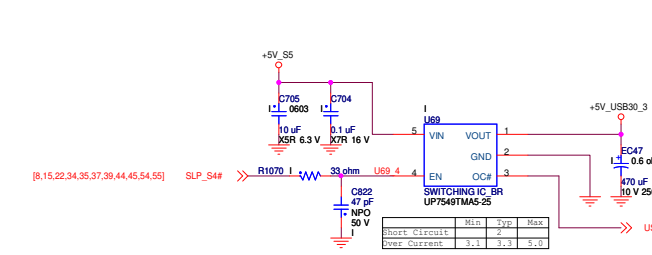
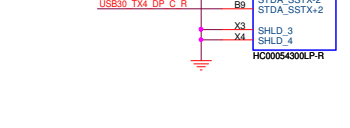
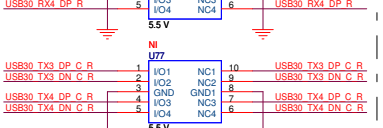
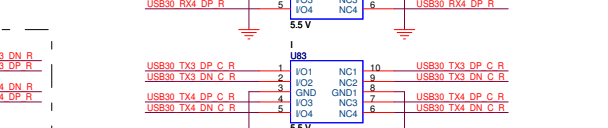
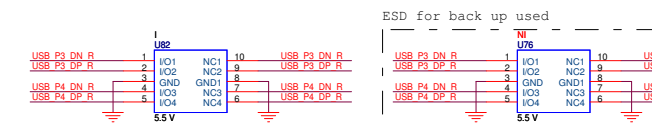
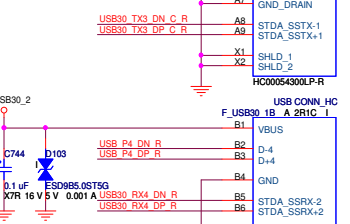
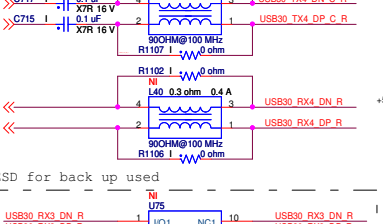
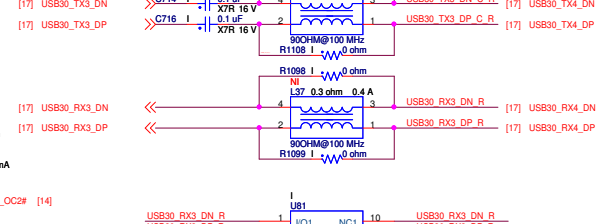
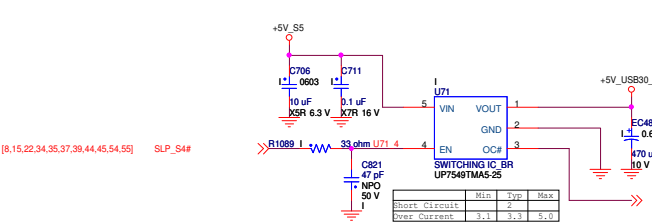
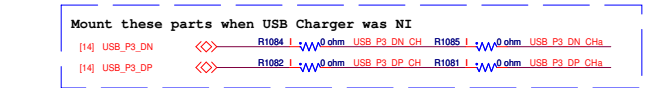
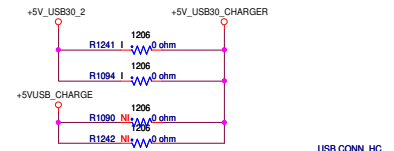
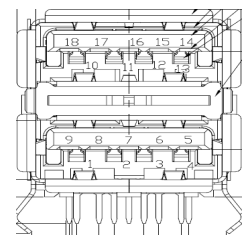


Front USB 3.0

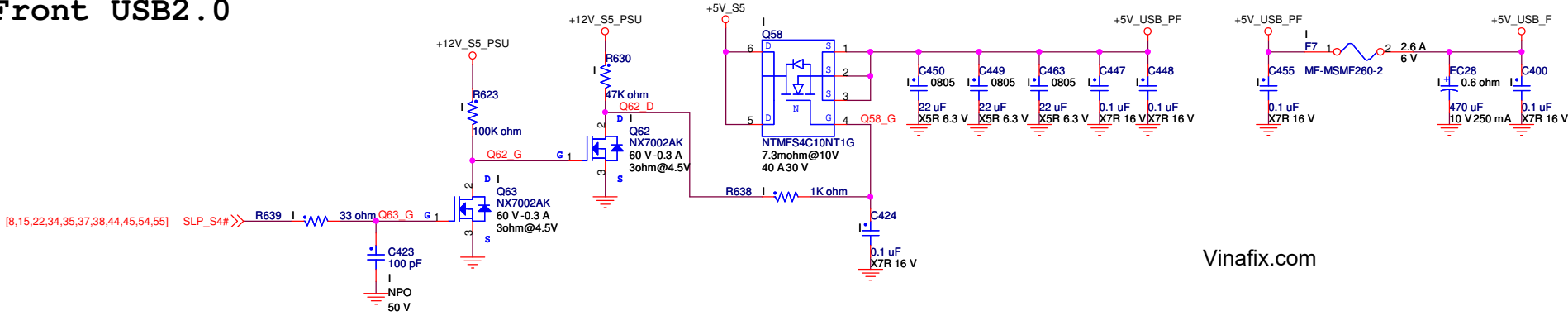
S0 : CDP 1.5A
S3 : CDP 1.5A
S4&S5 : DCP 2.3A



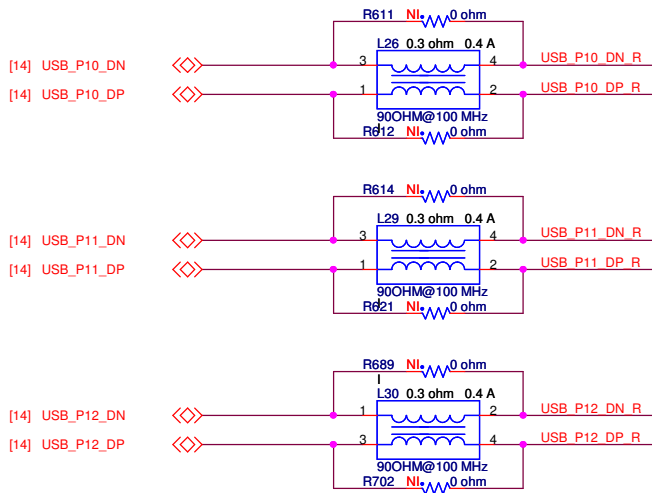
CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	Data Lines Disconnected
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected and Load Detect Function Active
0	0	1	1	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected and Load Detect Function Active
0	1	1	1	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	Charging Mode
1	1	0	0	SDP1	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	OFF	Data Lines Connected
1	1	1	0	SDP2 ⁽⁴⁾	ILIM_LO	OFF	Data Lines Connected and Load Detect Active
1	1	1	1	CDP ⁽⁴⁾	ILIM_HI	OFF	Data Lines Connected and Load Detect Active



Front USB2.0

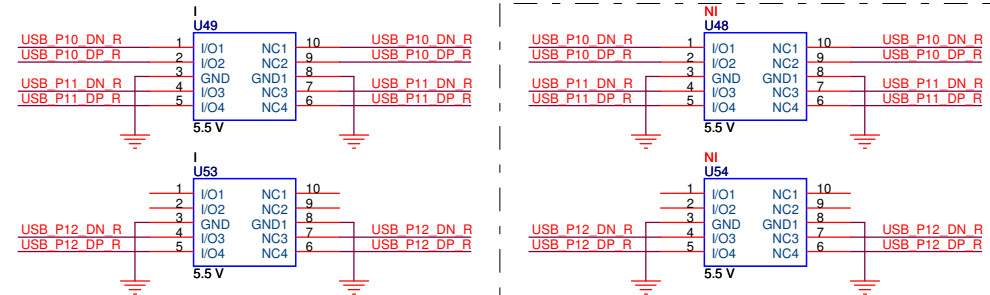
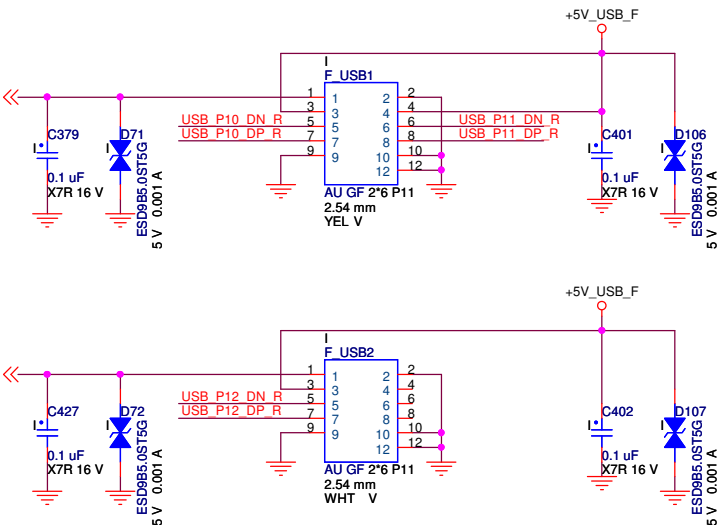


Vinafix.com



[15] FUSB_G1

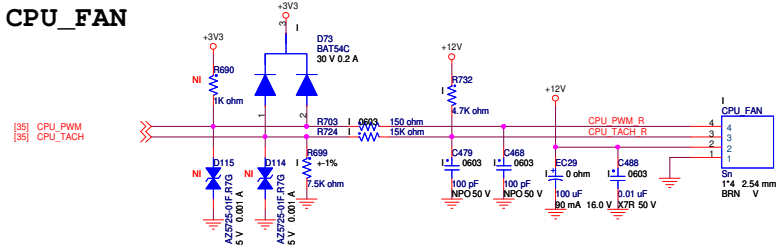
[15] FUSB_G2



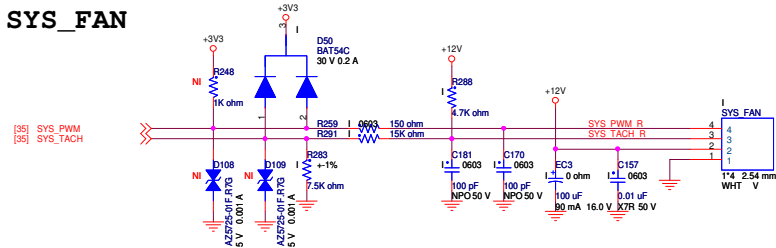
ESD for back up used

LITE-ON TECHNOLOGY CORP. LITEON		
Title		
39. USB2.0 Header		
Size	Document Number	Rev
B	MC117	X03
Date:	Wednesday, December 28, 2016	Sheet 39 of 58

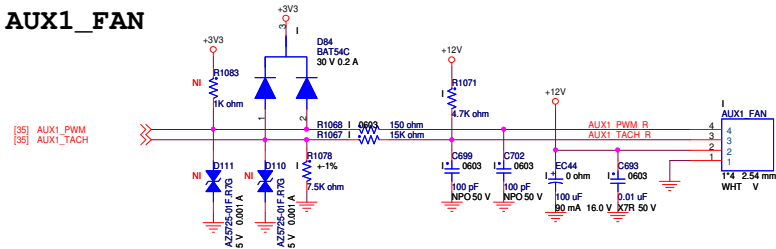
CPU_FAN



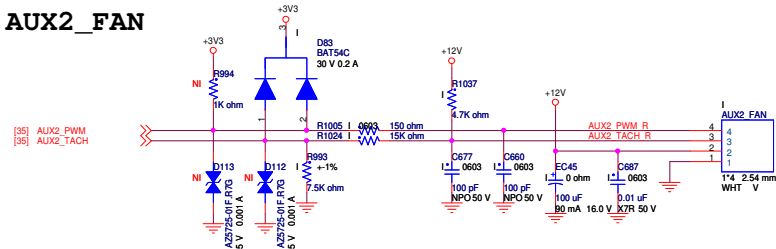
SYS_FAN



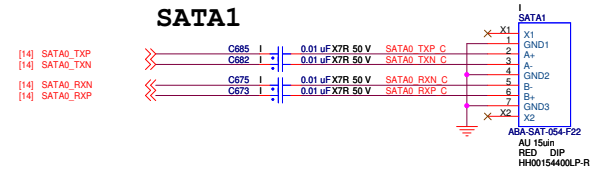
AUX1_FAN



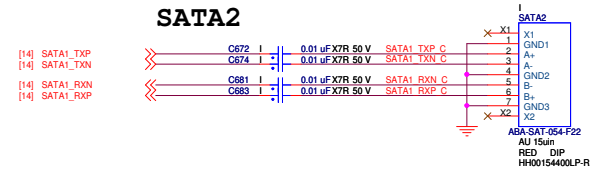
AUX2_FAN



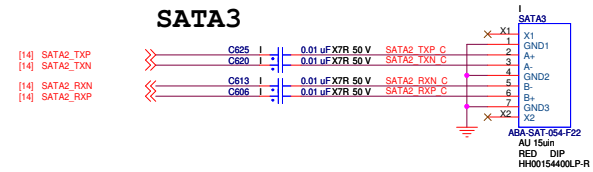
SATA1



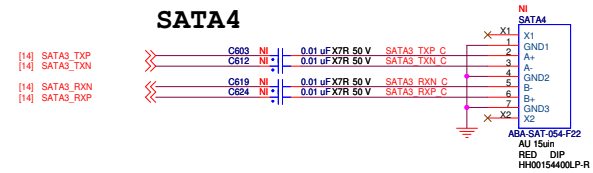
SATA2



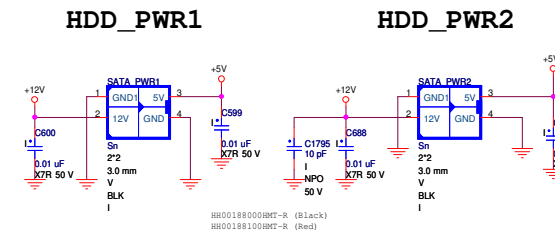
SATA3



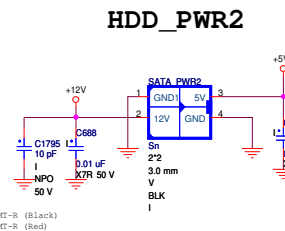
SATA4



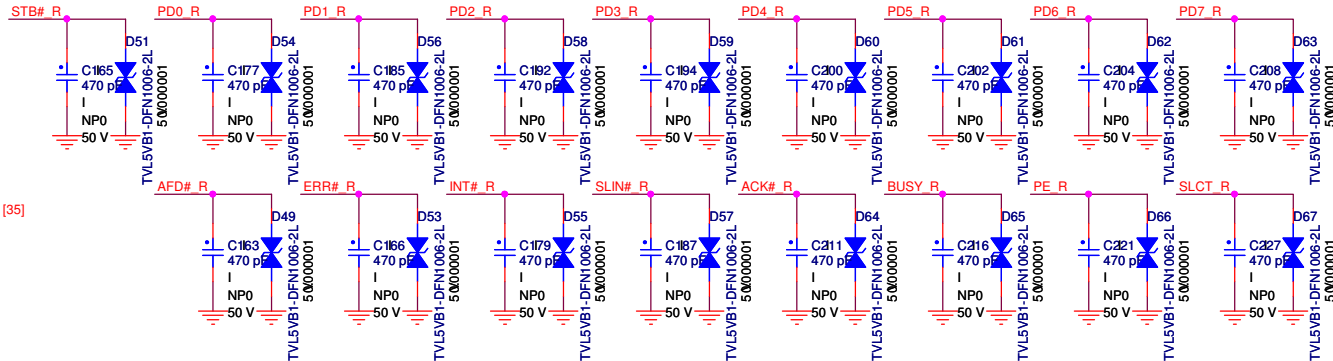
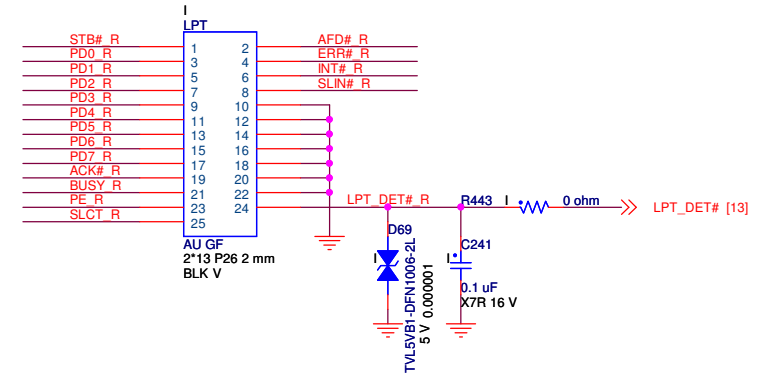
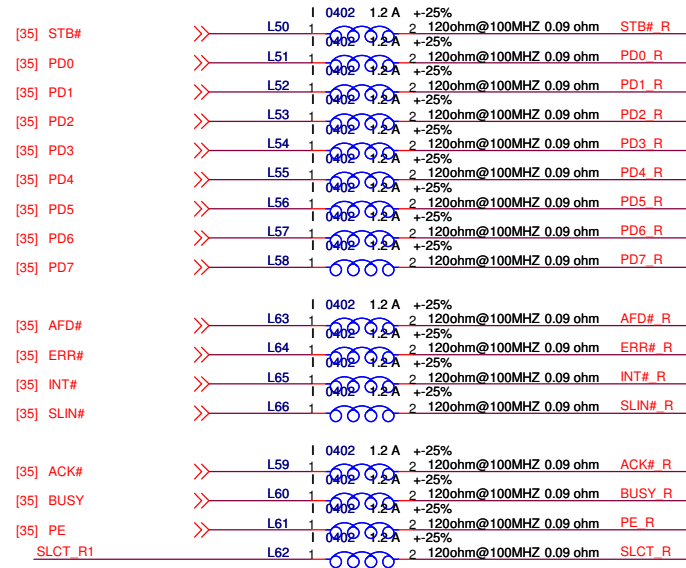
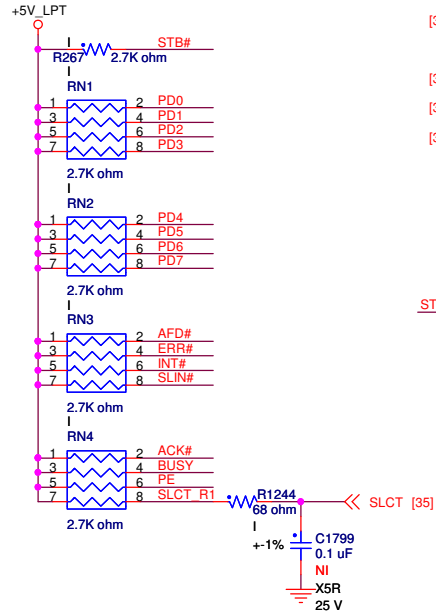
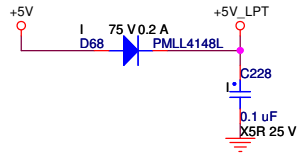
HDD_PWR1



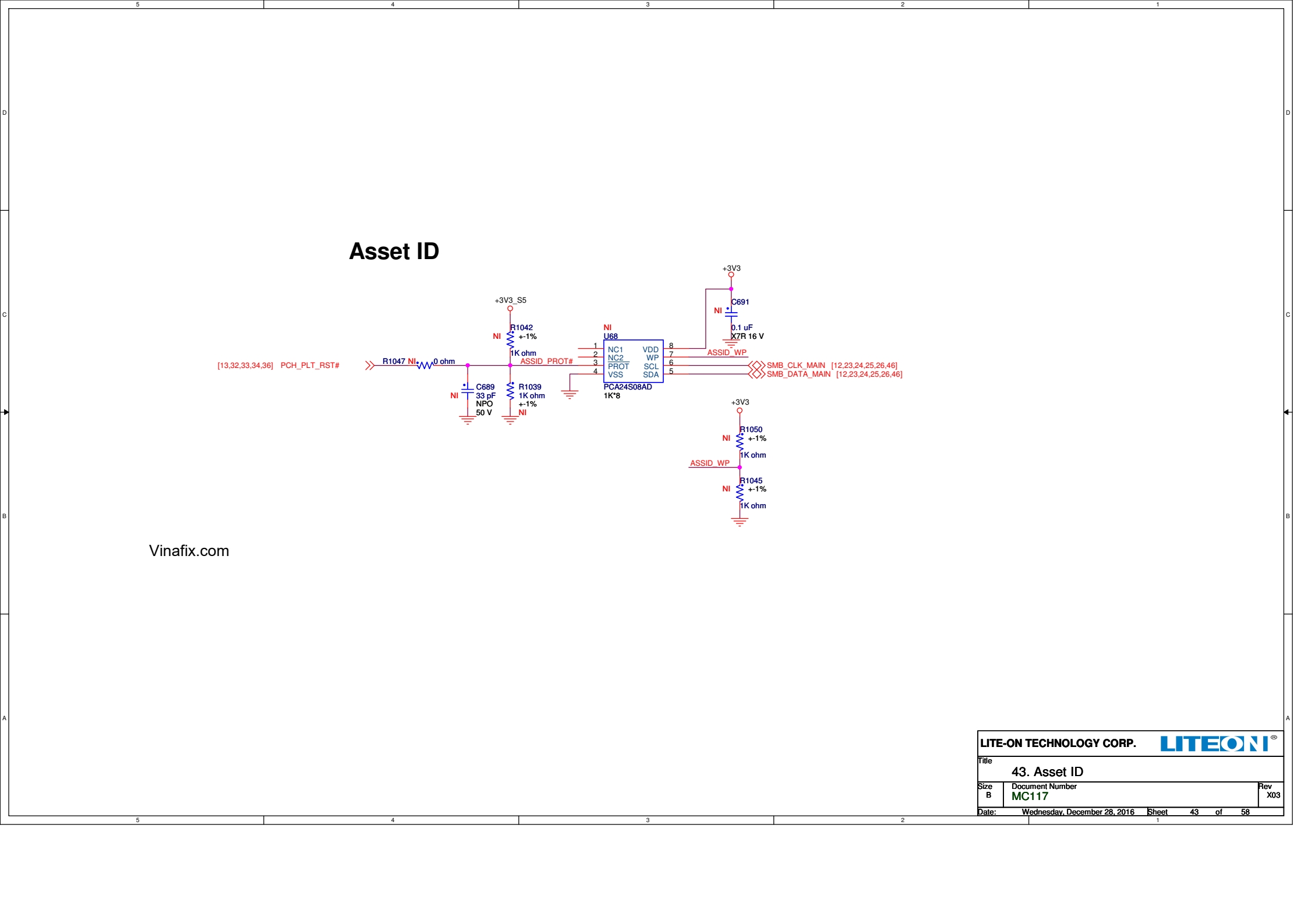
HDD_PWR2



PARALLEL PORT



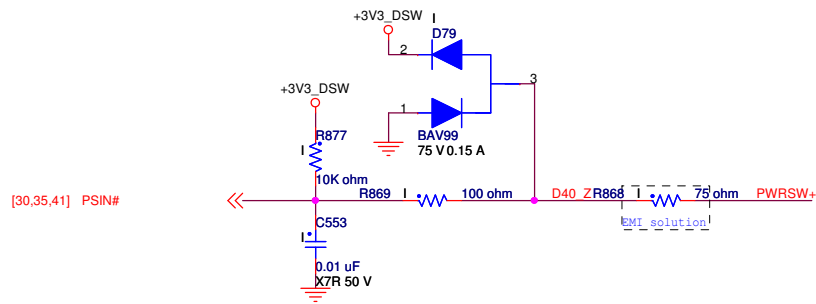
5	4	3	2	1
---	---	---	---	---



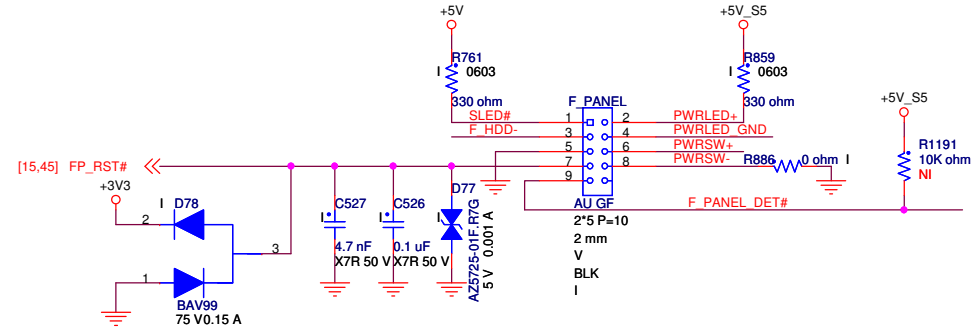
B

CONTROL PANEL / LED CIRCUITRY

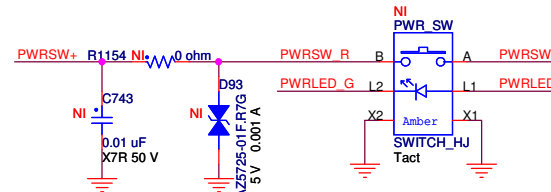
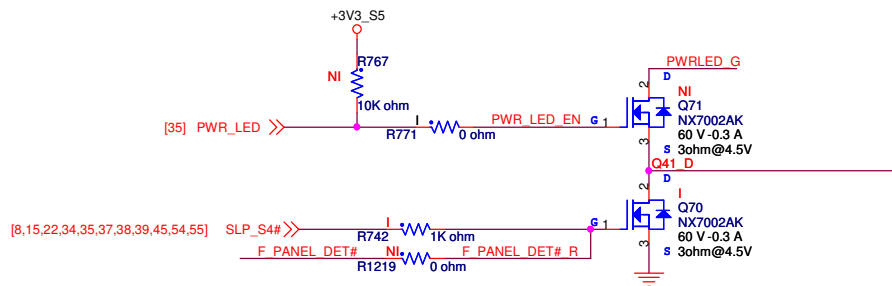
Power Button



Front Panel header

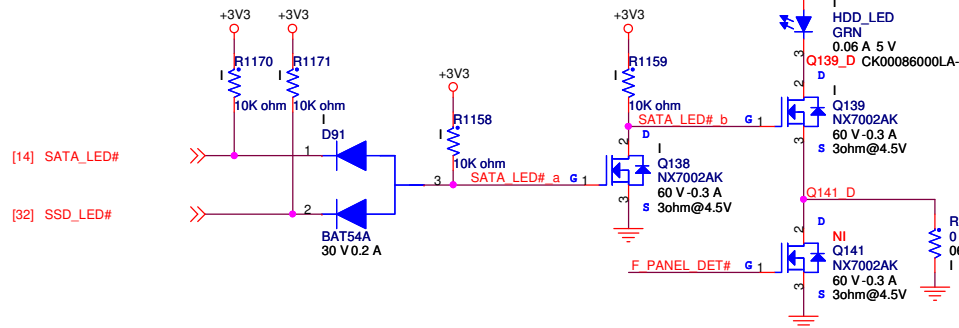


Power LED



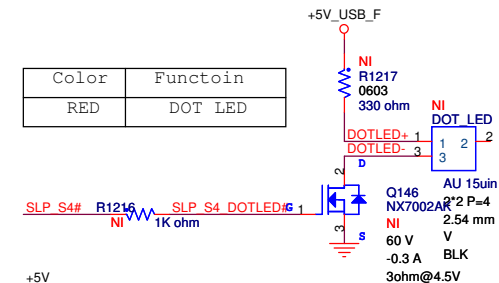
Power LED	
S0	LED is on steady green
S1 / S3	LED Blinks (1Hz/s)
S4 / S5	LED OFF

HDD LED

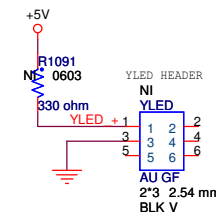


2016/6/30
Follow spec
Q70 , Q71 , Q141, R742 , R1219 , R1191 always NI
R1221 always I

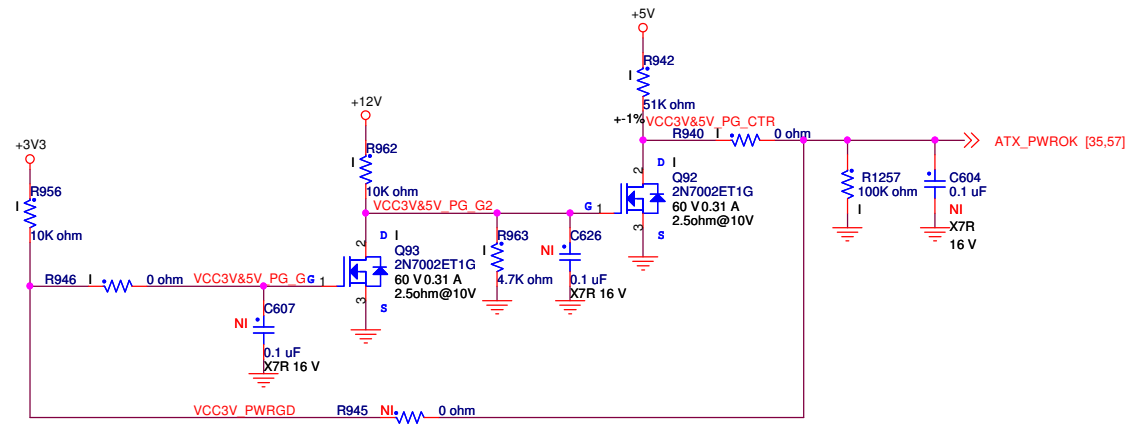
Color	Functoin
RED	DOT LED



Color	Functoin
G	PWR LED

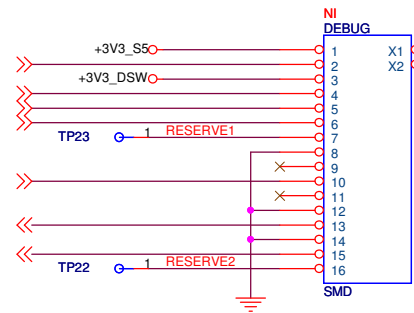


LITE-ON TECHNOLOGY CORP. LITEON®	
Title	
44. Button/LED	
Size B	Document Number MC117
Date:	Wednesday, December 28, 2016
Sheet	44 of 58



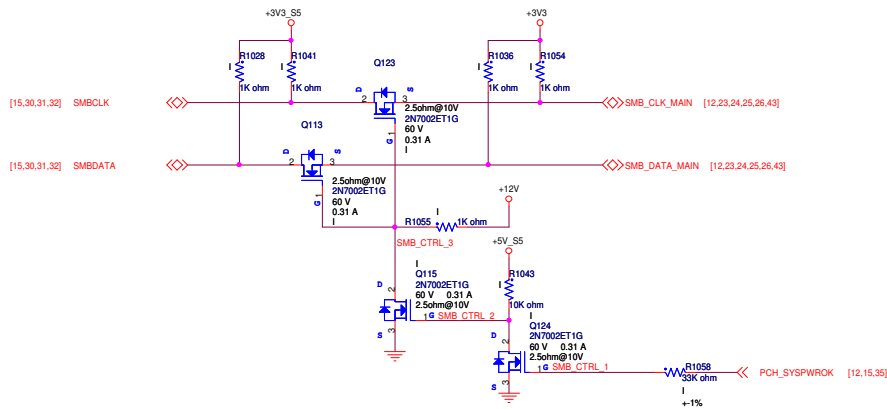
For APS test

[15,22,30,35,46,54] SLP_S3#
 [15] SLP_S5#
 [8,15,22,34,35,37,38,39,44,54,55] SLP_S4#
 [15] SLP_A#
 [15] APS_RTCSRST#
 [12,15,35] PWRBTN#
 [15,44] FP_RST#



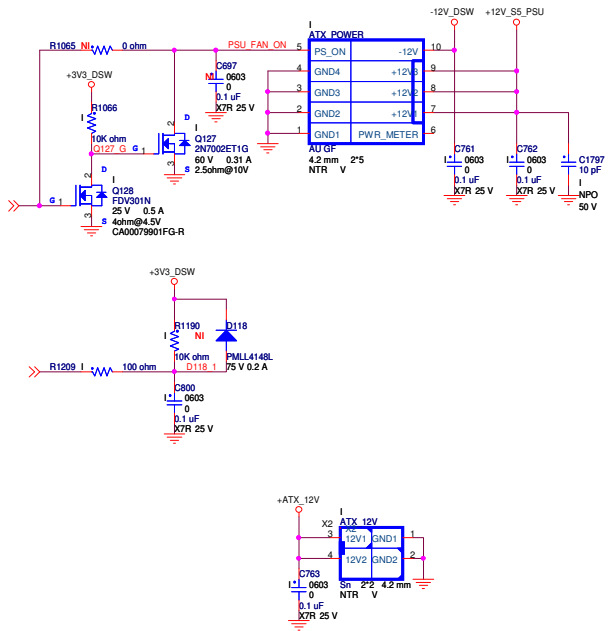
LITE-ON TECHNOLOGY CORP. LITEON [®]		
Title		
45. APS Debug Port/ATX PWROK		
Size	Document Number	Rev
B	MC117	X03
Date:	Wednesday, December 28, 2016	Sheet 45 of 58

SM Bus



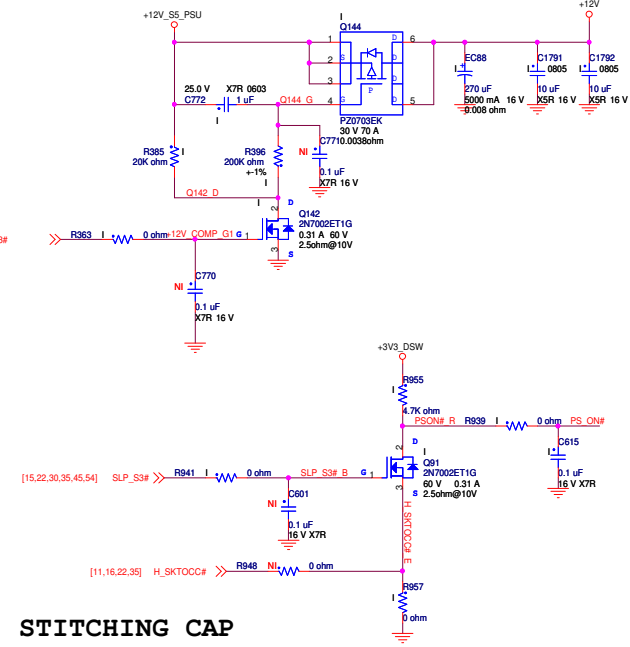
[22,35,48,50] PS_ON#

[22,35,48,50] PS_ON#



Imax: 14A

[15,22,30,35,45,54] SLP_S3#



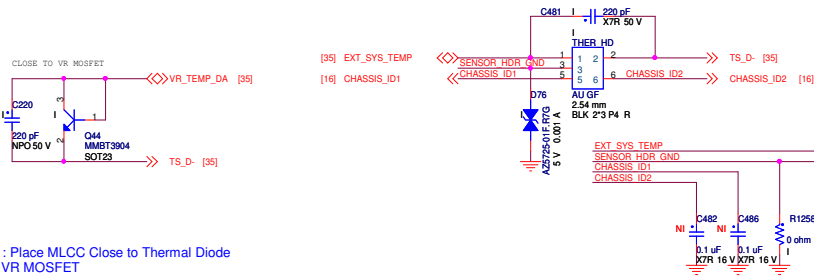
STITCHING CAP

LITE-ON TECHNOLOGY CORP. LITEON®			
File			
46. SM BUS/Thermal Sensing/ATX			
Size	Document Number	Rev	
C	MC117	X03	
Date:	Wednesday, December 28, 2016	Sheet	46 of 58

Temperature Sensing

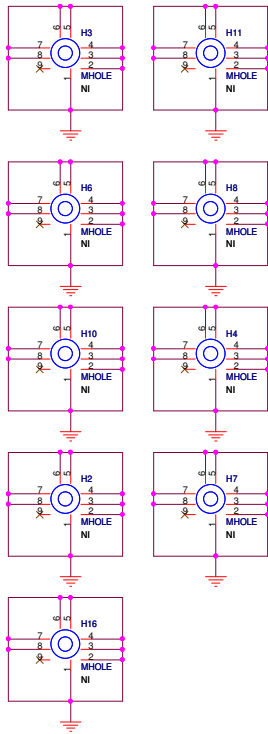
Current Mode

SYS THERMAL SENSOR



CAD NOTE : Place MLCC Close to Thermal Diode
CLOSE TO VR MOSFET

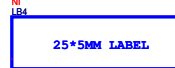
Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconductor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSC



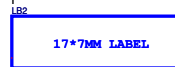
BAR CODE Label



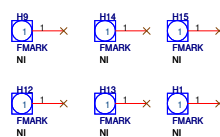
FRU Label



LAN Label



AMI Label



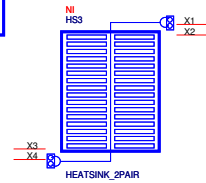
PCB



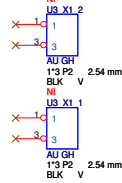
CPU metal



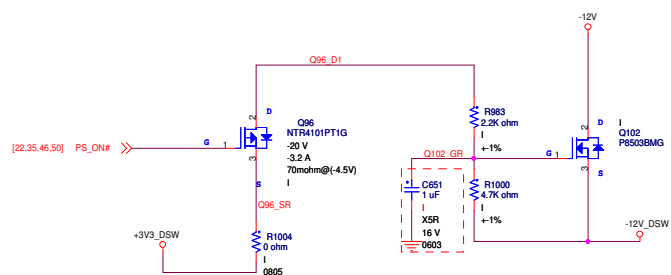
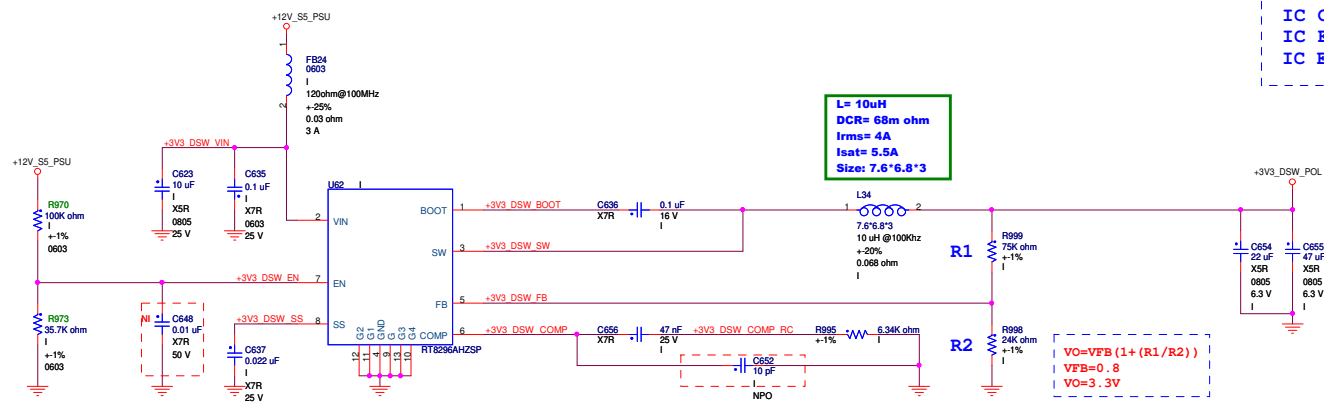
PCH HS



PCH HS DUCT



Vinafix.com

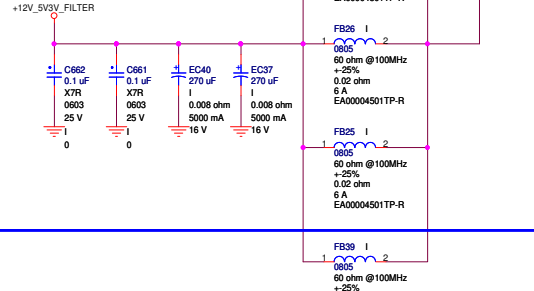


+5V_S5

Vin:12V_5V3V_FILTER
Vout:+5V_S5
Max Load: 17.28A
OCP Min: 25.92A
Fsw:300KHz(typ)
IC EN1 ON > 1.6 V
IC EN1 OFF < 0.4 V

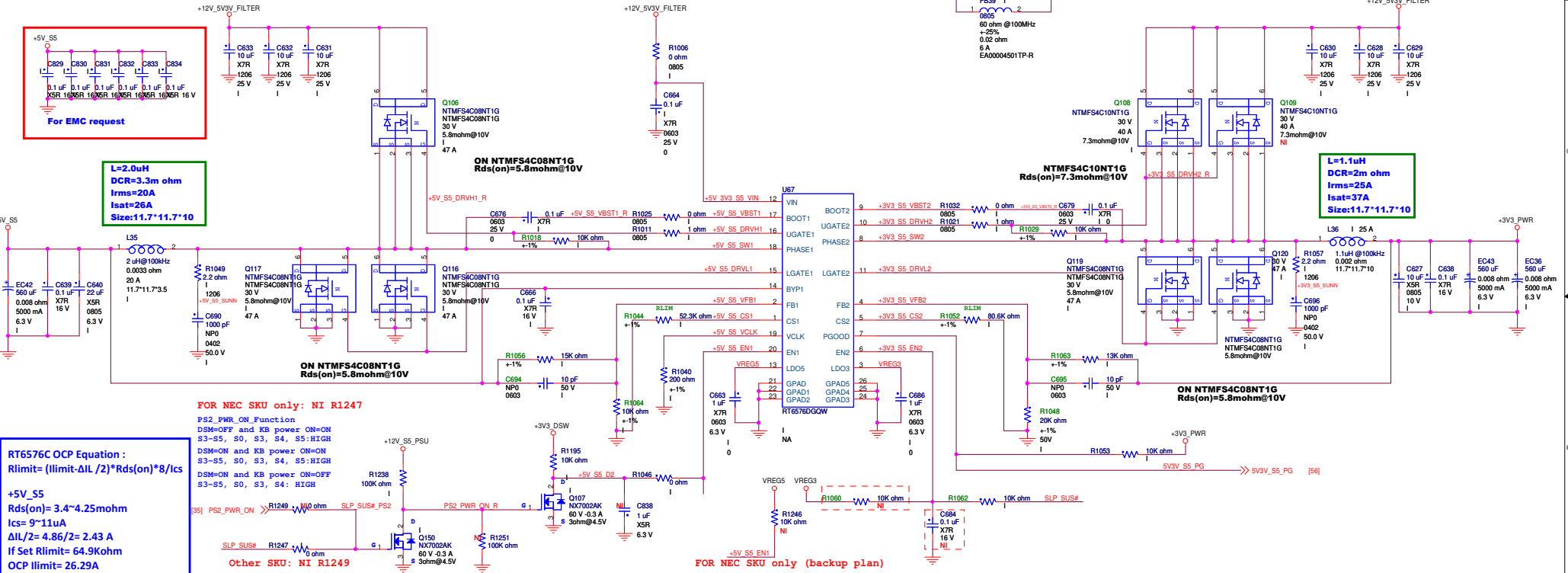


+5V3V_VIN_FILTER



+3V3_PWR

Vin:12V_5V3V_FILTER
Vout:+3V3_S5
Max Load:24.12A
OCP Min:36.18A
Fsw:355KHz(typ)
IC EN2 ON > 1.6 V
IC EN2 OFF < 0.4 V



MLCC Ripple current=1.5A

+12V_5V3V_FILTER:
Cin= 600uF(EC+MLCC)
Ripple current= 19A

+5V_S5:
Cout= 582uF(EC+MLCC)
Ripple current= 6.5A

+3V3_S5:
Cout= 1164uF(EC+MLCC)
Ripple current= 13A

+5V_S5 LIR
= $\Delta I_L / I_{max}$
= 4.86/17.28
= 0.281

+3V3_S5 LIR
= $\Delta I_L / I_{max}$
= 6.13/24.12
= 0.254

使用RT6576(+3V3_DSW)
1. FB28-->NI
2. FB29,FB30,R1062-->NI
3. FB31,R1060-->ADD
4. R947,Q99,C649-->ADD

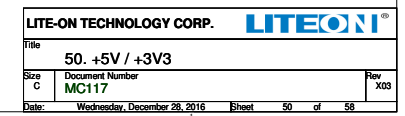
使用RT8296A(+3V3_DSW)-----Default
1. FB28-->Add
2. FB29,FB30,R1062-->Add
3. FB31,R1060-->NI
4. R947,Q99,C649-->NI

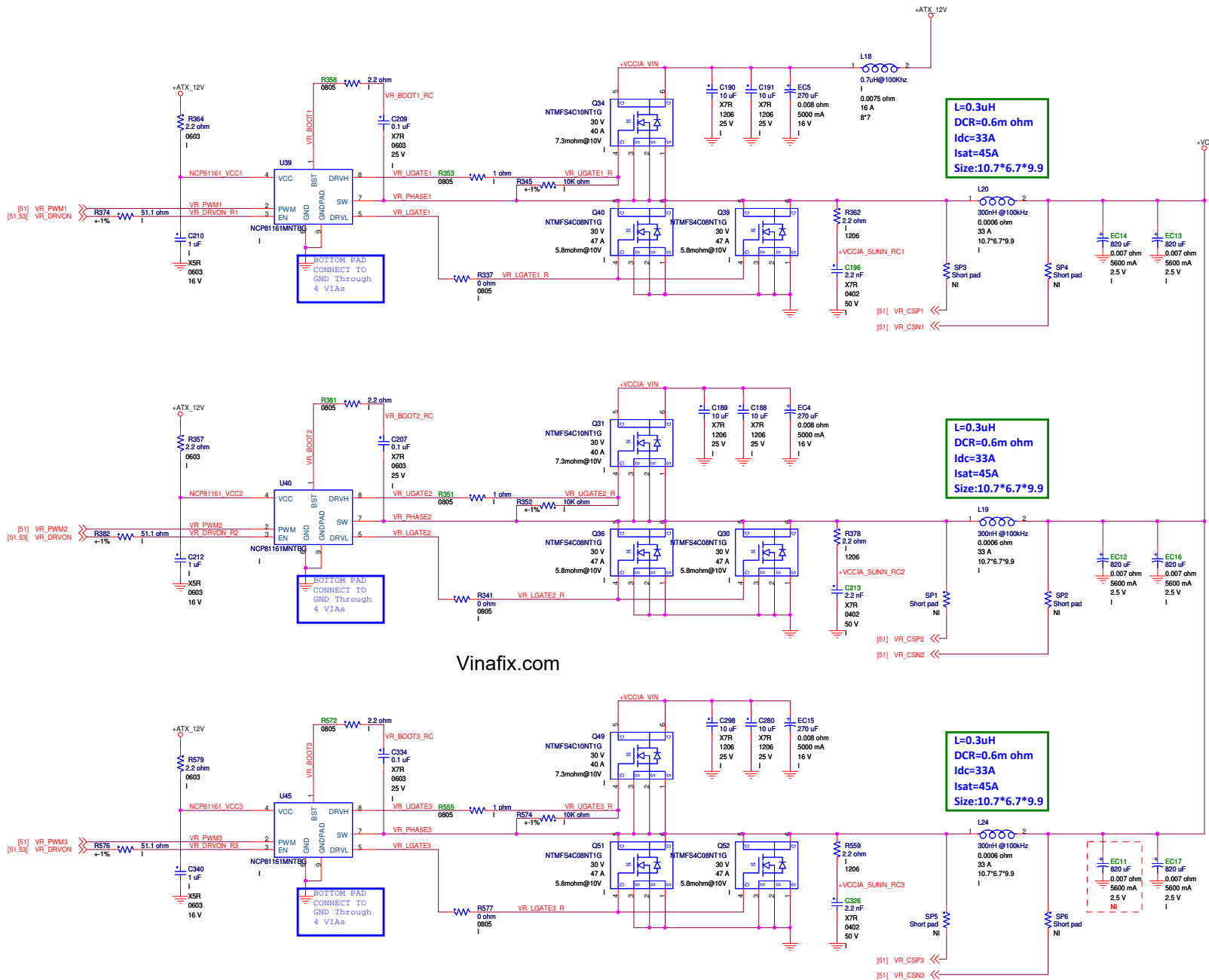
+3V3_S5
+3V3_S5 @Imax 7.43A
Soft start:2.519ms
Inrush current:166.6mA

Please Check
IC EN ON > 1.6V
IC EN OFF < 0.4V

RT6576C OCP Equation :
 $R_{lim} = (I_{limit} - \Delta I_L / 2) * R_{ds(on)} * 8 / I_{cs}$

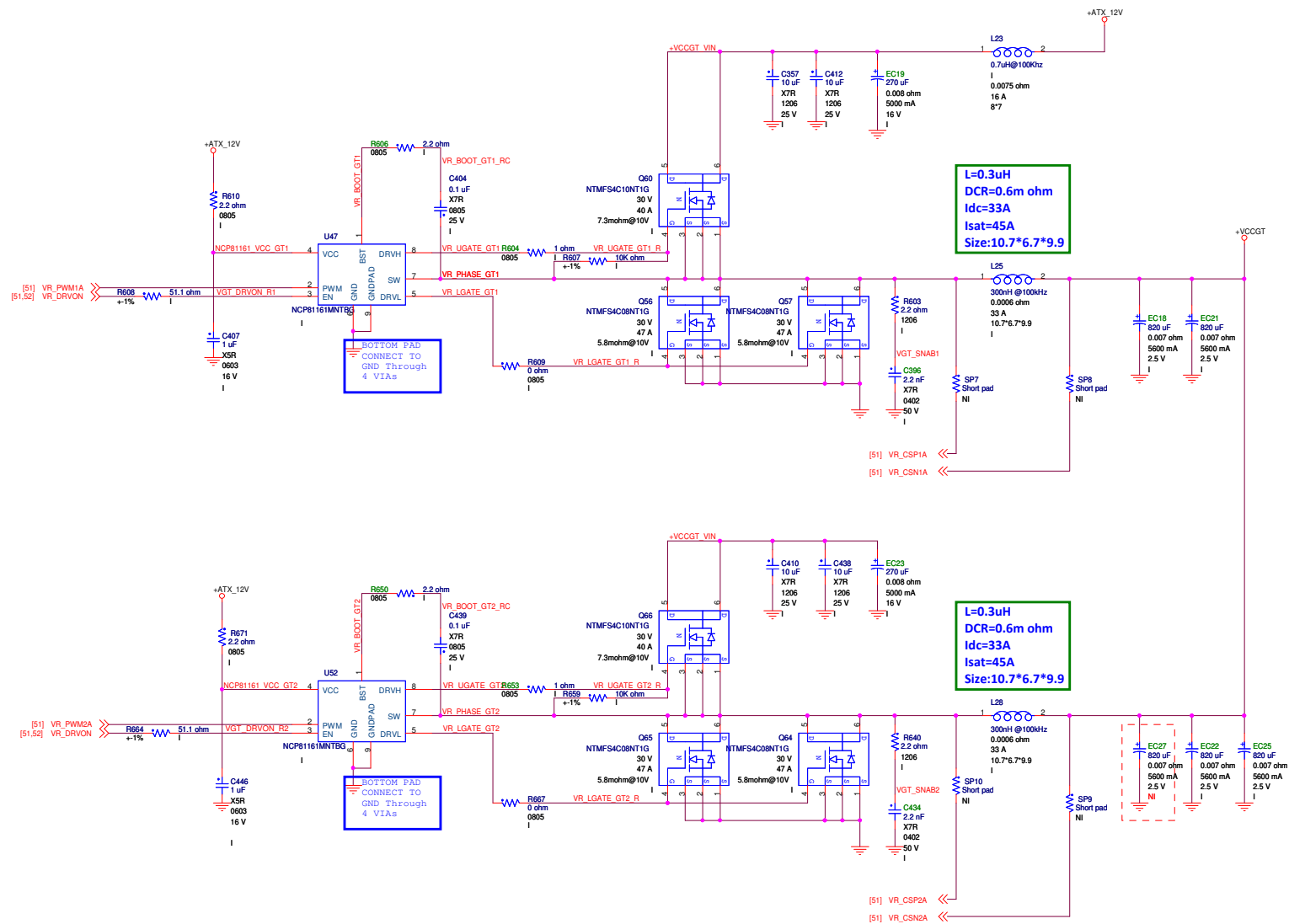
+3V3_S5
Rds(on)= 3.4~4.25mohm
Ics= 9~11uA
 $\Delta I_L / 2 = 6.13 / 2 = 3.065 A$
If Set Rlimit= 90.9Kohm
OCP Ilimit= 36.48A

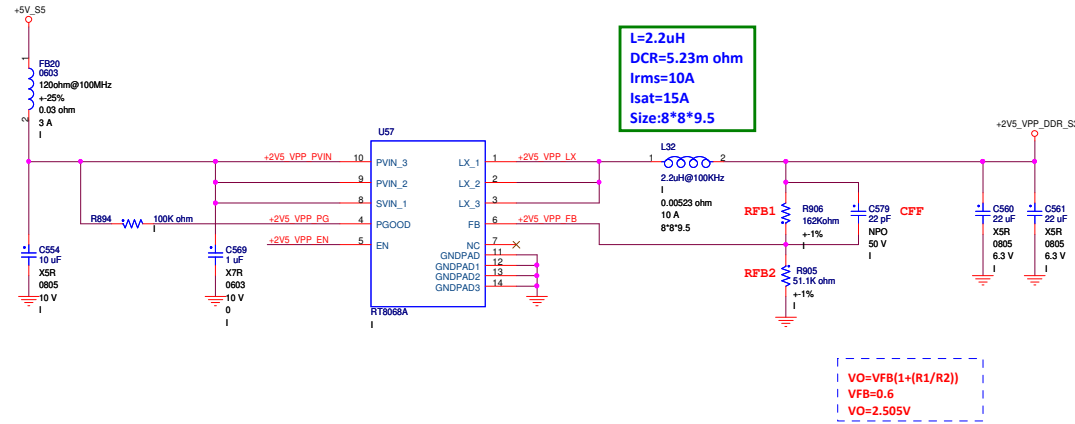




Vinafix.com

+VCCIA
 Vin: +12V_CPU
 Vout: +VCCIA
 DC Loadline: 2.1mohm
 ITDC: 61A
 Imax: 79A

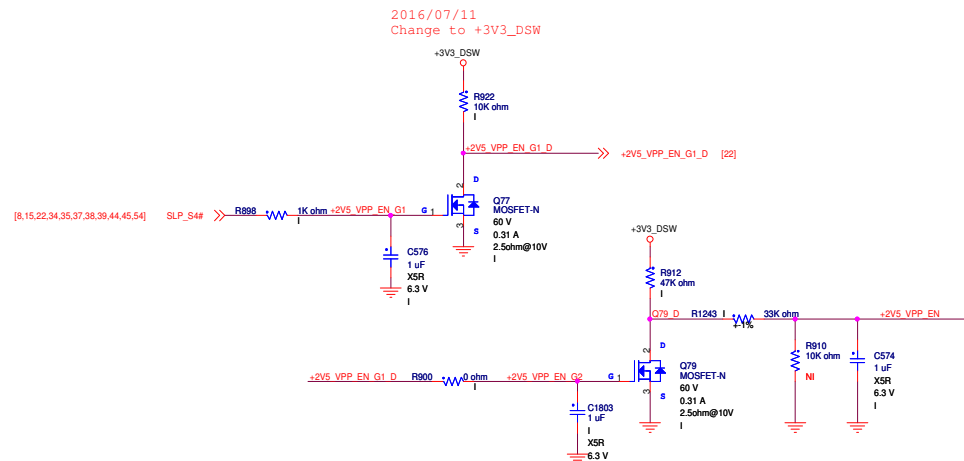


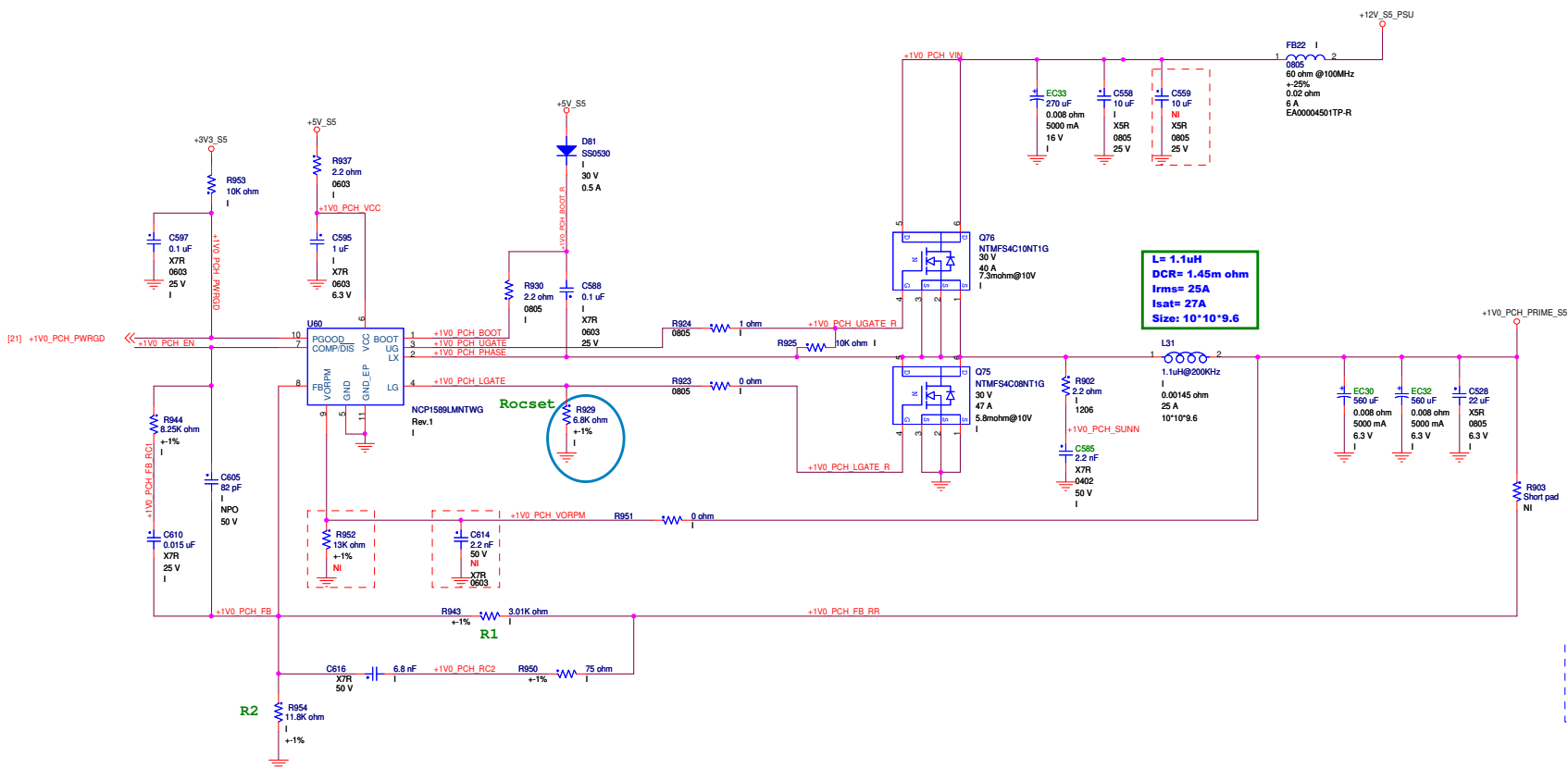


+2V5_VPP_DDR_S3
 Temp. Max. DC: 2.4A
 OCP: 4A(typ)
 IC EN ON > 1.6 V
 IC EN OFF < 0.4 V
 Fsw: 1MHz

Table 1. Recommended Component Selection

VOUT (V)	RFB1 (kΩ)	RFB2 (kΩ)	CFF (pF)	L (μH)	COUT (μF)
3.3	229.5	51	22	2	22 x 2
2.5	161.5	51	22	2	22 x 2
1.8	102	51	22	1.5	22 x 2
1.5	76.5	51	22	1.5	22 x 2
1.2	51	51	22	1.5	22 x 2
1.0	34	51	22	1.5	22 x 2





+1V0_PCH
 $I_{max} = 7.5A$
 $OCP_{Min} = 11.25A$
 $IC_{EN\ ON} > 1.3\ V$
 $IC_{EN\ OFF} < 0.7\ V$
 $F_{sw} = 320KHz$

+12V_S5_PSU:
 $C_{in} = 280uF$ (MLCC + EC CAP)
 CAP Ripple current= 6A
+1V0_PCH:
 $C_{out} = 1142uF$ (EC+MLCC)
 CAP Ripple current= 11A

+1V0_PCH_PRIME_S5 LIR
 $= \Delta IL / I_{max}$
 $= 2.6 / 7.5$
 $= 0.34$

$V_{out} = (1+R1/R2) * 0.8 = 1.004V$
 $OCP = 9.5uA * Rocset / L-S\ Rds(on)$
 $= (9.5uA * 11.8K) / 8.5m$
 $= 13.18A$

EE Check Enable

Please Check
 $IC_{EN\ ON} > 1.3\ V$
 $IC_{EN\ OFF} < 0.7\ V$

[15,21,22,35,49] SLP_SUS# >> R926 1K ohm

[49] 5V3V_SS_PQ >> R1213 NI 0 ohm

2016/09/01

If change to new design
 Mount R926 , NI R1213

